

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
			2010-08-05

SCHEM, FLYING_CLOUD, MLB, K90i

" EVT3 "

11/22/10

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ALIASES RESOLVED


Schematic / PCB #'s

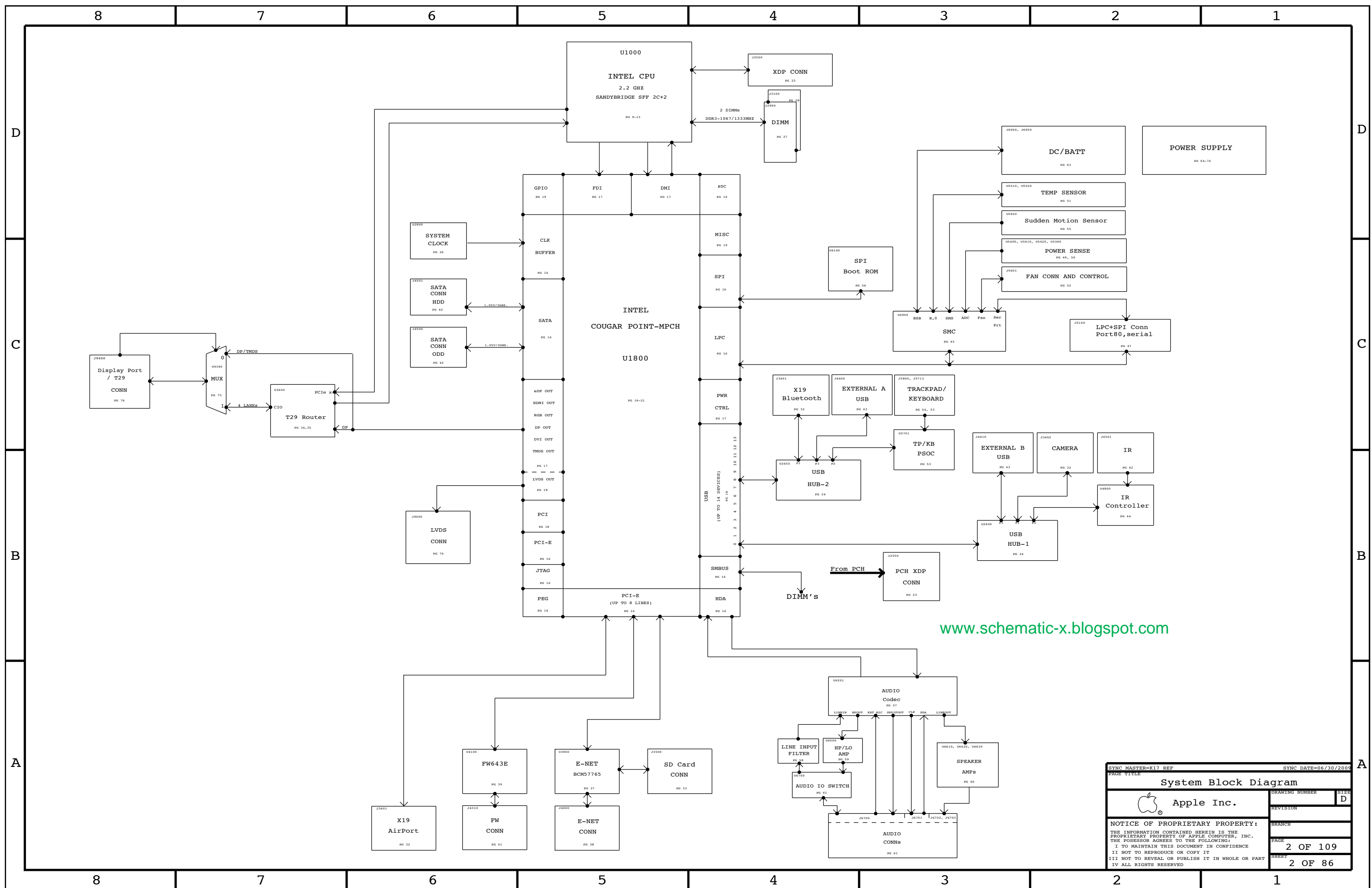
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8658	1	SCHEM,MLB,K901	SCH	CRITICAL	
820-2936	1	PCBF,MLB,K901	PCB	CRITICAL	

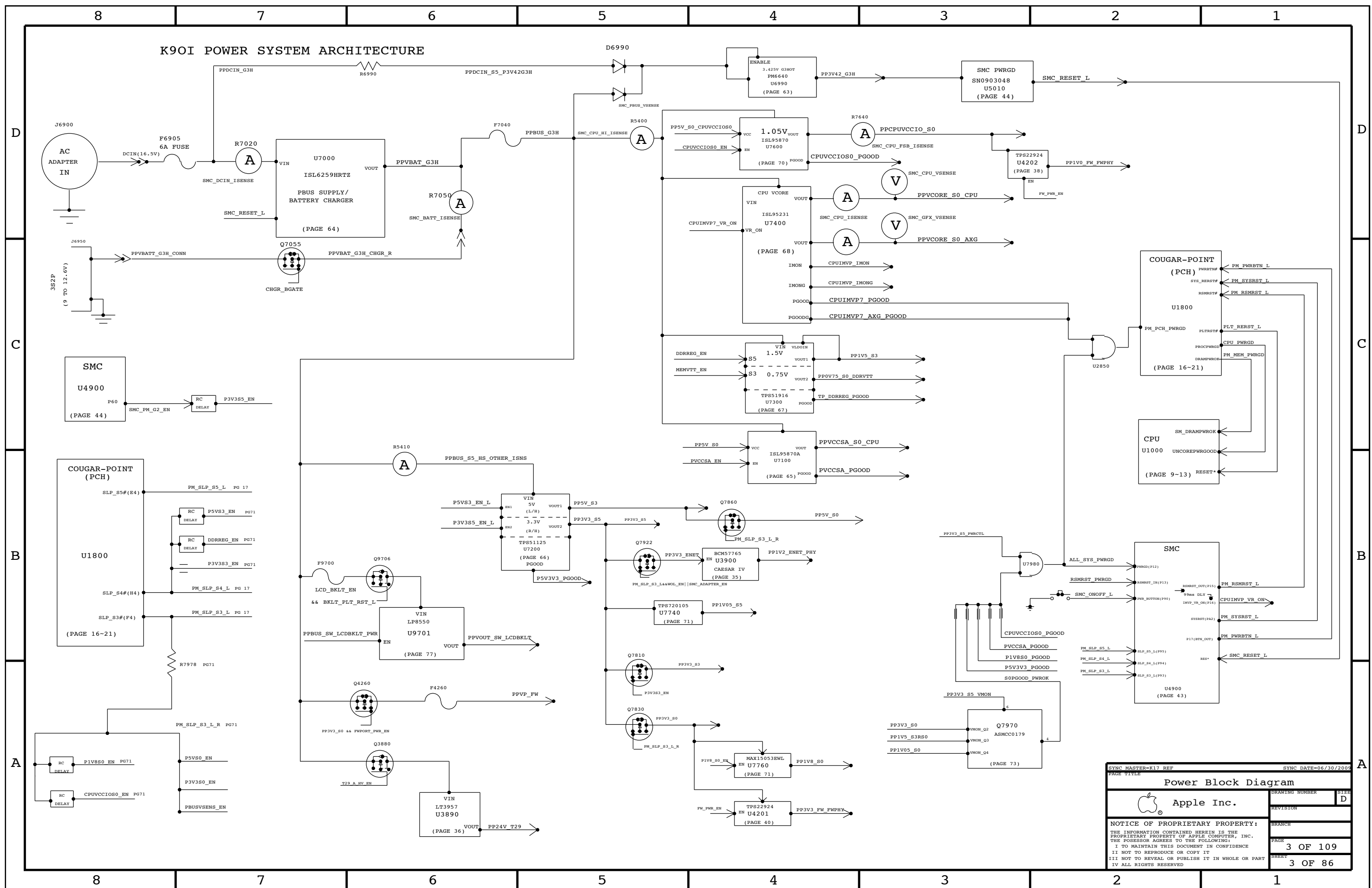
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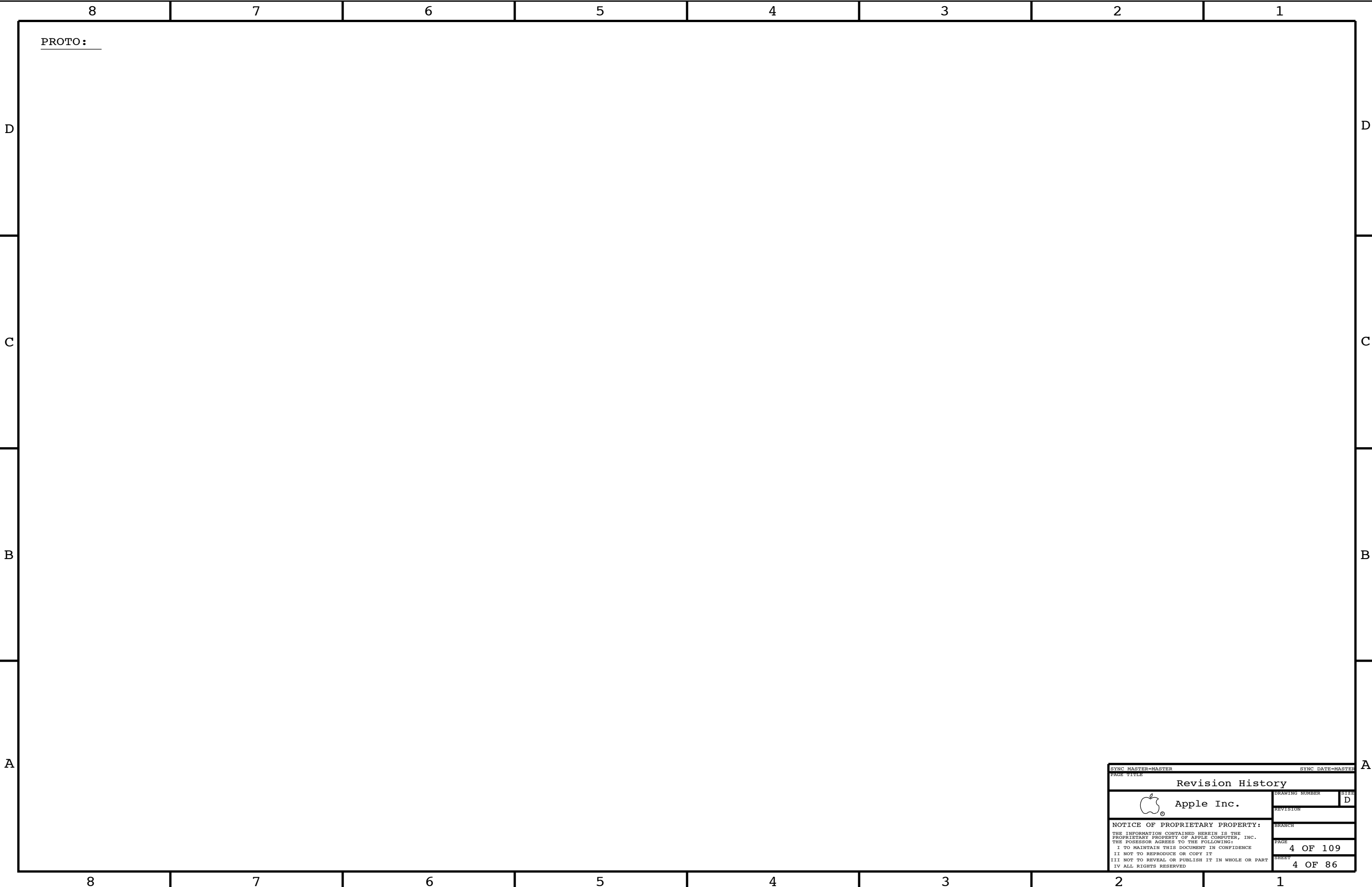
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PROTO:

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SYNC DATE=MASTER

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Revision History

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1294	PCBA, 2.5G, K90i	K90i_COMMON, CPU_2_5GHZ, EEEF_DDRQ
639-1581	PCBA, 2.7G, K90i	K90i_COMMON, CPU_2_7GHZ, EEEF_DN78
639-1698	PCBA, 2.6G, K90i	K90i_COMMON, CPU_2_6GHZ, EEEF_DHB8
639-1699	PCBA, 2.3G, K90i	K90i_COMMON, CPU_2_3GHZ, EEEF_DHG8
085-1998	K90i MLB DEVELOPMENT BOM	K90i_DEVEL:ENG

K90i BOM GROUPS

BOM GROUP	BOM OPTIONS
K90i_COMMON	ALTERNATE,COMMON,K90i_COMMON1,K90i_COMMON2,K90i_DEBUG:ENG,K90i_PROGPARTS,USBHUB_2513B,T29BST:Y
K90i_COMMON1	BATT_3S,CPUMEM_S0,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_3NONREM,T29:YES,DP_SDRV:A2,SDRV_DP,SDRV12C:MCU
K90i_COMMON2	MIKEY,KB_BL
K90i_PROGPARTS	BOOTROM_PROG,SMC_PROG,TPAD_PROG,ENET_PROG,T29ROM:PROG,T29MCU:PROG
K90i_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCPLUS,VREFMRGN,SOPGOOD_ISL,INVPISNS_ENG
K90i_DEVEL:PVT	LPCPLUS,XDP_CONN,XDP_PCH
K90i_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K90i_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT
K90i_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT,LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33783934	1	SNB,2C,0XXX,RS1,2,2,35W,R2,3M,GT1,BGA	U1000	CRITICAL	CPU_2_2GHZ
33784058	1	SNB,Q1RA,QS,J1,2,5,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_5GHZ
33784057	1	SNB,Q1R3,QS,J1,2,7,35W,2+2,1.30,4M,BGA	U1000	CRITICAL	CPU_2_7GHZ
33784024	1	SNB,Q1R9,QS,J1,2,3,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_3GHZ
33784064	1	SNB,Q1R7,QS,J1,2,6,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_6GHZ
33784029	1	IC,PCB,COG8ARPO13PT,SLH9D,PQ0,B082BH65	U1800	CRITICAL	
34380534	1	IC,BCH57765B0,ENET&D,BX8	U3900	CRITICAL	
33880753	1	IC,PW643-02,1394B PWR/MCCT LINE/PC1-0,12	U4100	CRITICAL	
33880921	1	IC,T29-C0,220 FCBCGA,15x15MM	U3600	CRITICAL	T29:YES
35383055	1	IC,P13VEDP212,X2 DISPLAYPORT 2+1 MUX,QFN	U9390	CRITICAL	

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0663	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,RP,80IC	U3990	CRITICAL	ENET_BLANK
341S3026	1	IC ENET,11MBITFLAN,CIV REV01,K60/K62	U3990	CRITICAL	ENET_PROG
335S0777	1	IC,EEPROM,SERIAL,SPI,1Kx8,1.8V,MLP8,LF	U3690	CRITICAL	T29ROM:BLANK
341T0317	1	IC,T29 ASSY	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2939	1	IC,PROGMD,LPC1112A,T29 PORT MCU,HVQFN25	U9330	CRITICAL	T29MCU:PROG
338S0895	1	IC,SMC,NS8/2117/99MX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341T0300	1	IC,SMC,K901	U4900	CRITICAL	SMC_PROG
335S0770	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
335S0769	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341T0299	1	IC,EFI ROM,K901	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IS,ENCORE II, CY7C63803-LQMC	U4800	CRITICAL	
341S3024	1	IC,TP PSOC,K90,K901,K91,K91F,K92	U5701	CRITICAL	TPAD_PROG

Development BOM


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1998	1	K901 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

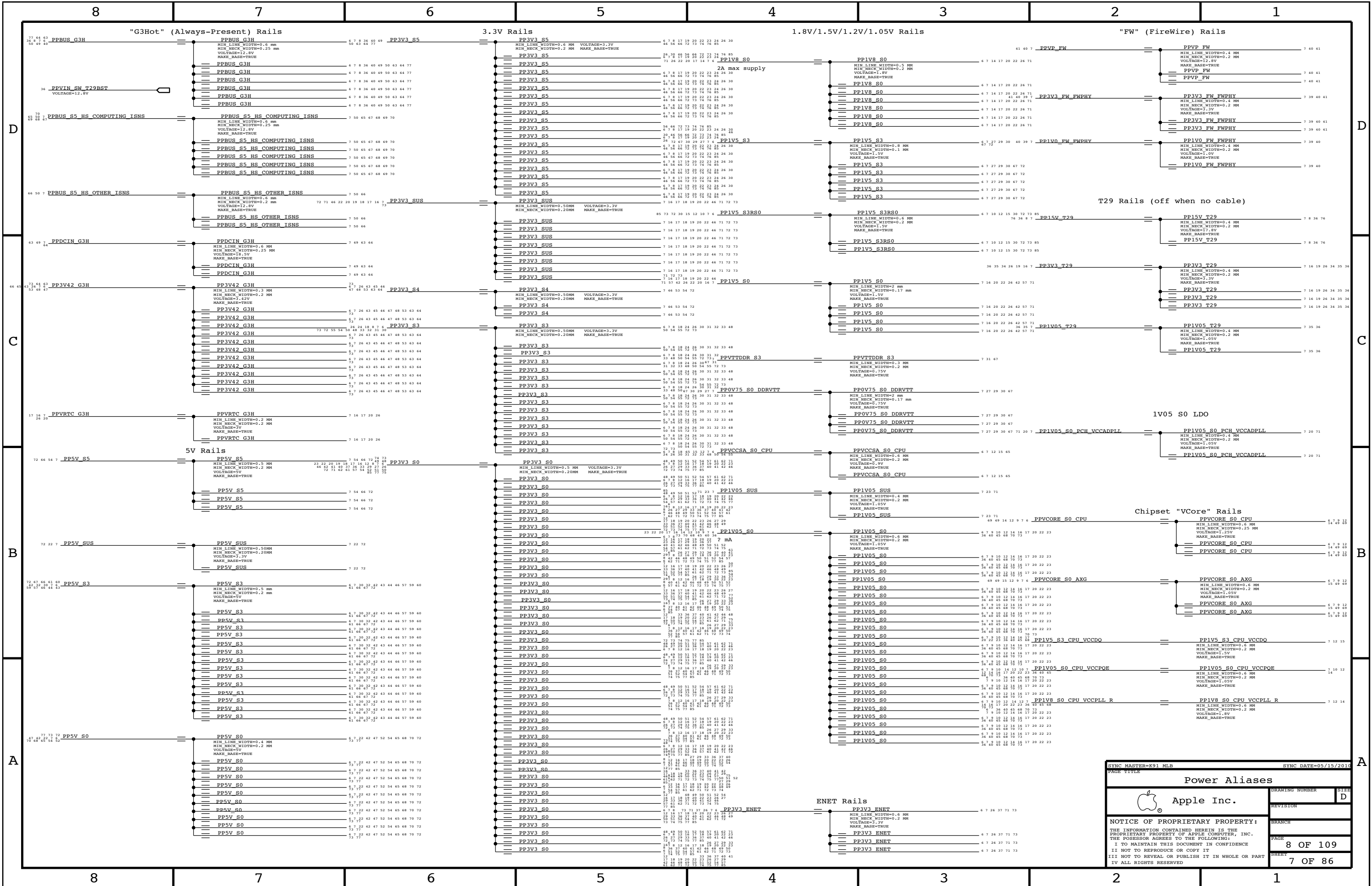
Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DDRQ]	CRITICAL	EEEE_DDRQ
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DH78]	CRITICAL	EEEE_DH78
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DH8F]	CRITICAL	EEEE_DH8F
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DH8G]	CRITICAL	EEEE_DH8G

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
15780058	15780055		ALL	Delta alt to TDK Magnetics
516S0805	516S0806		ALL	Hulex alt to Picoconn
128S0303	128S0282		ALL	Panasonic alt to Sanyo
138S0676	138S0691		ALL	Murata alt to Samsung
15280778	15280693		ALL	Cytec alt to Vishay
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
376S0927	376S0966		ALL	Fairchild alt to Renesas
376S0927	376S0790		ALL	Fairchild alt to CIRCLOW
376S0960	376S0801		ALL	Renesas alt to Renesas
376S0790	376S0928		ALL	CIRCLOW alt to Fairchild
376S0928	376S0895		ALL	Fairchild alt to Renesas
376S0937	376S0845		ALL	Fairchild alt to Renesas
376S0757	376S0761		ALL	ADN alt to Siliconix
376S0957	376S0958		ALL	Fairchild alt to Fairchild
376S0953	376S0958		ALL	Fairchild alt to Renesas
35383085	35381658		ALL	STMicro alt to LT

SYNC MASTER=K17 REF		SYNC DATE=05/28/2005	
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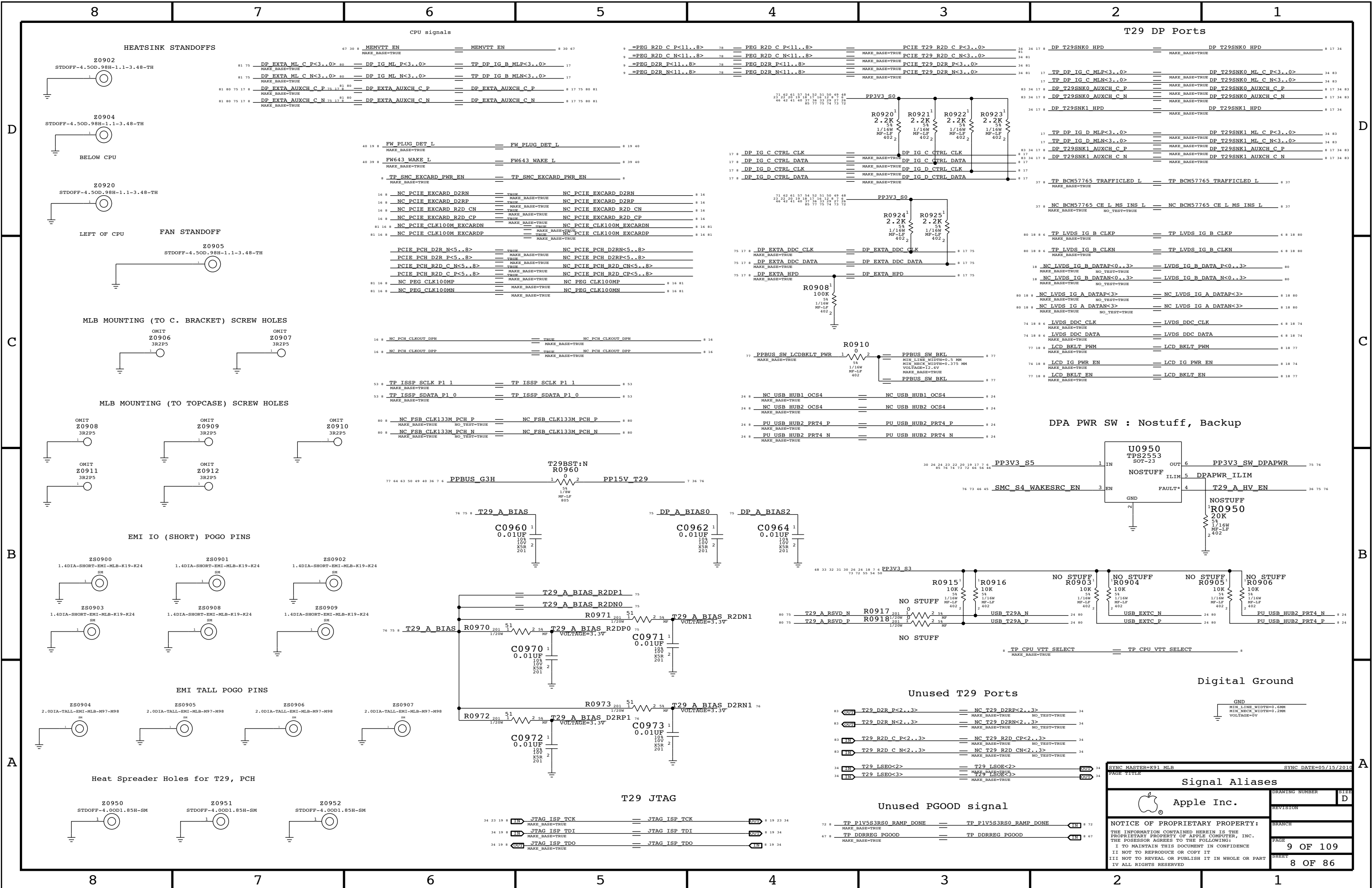
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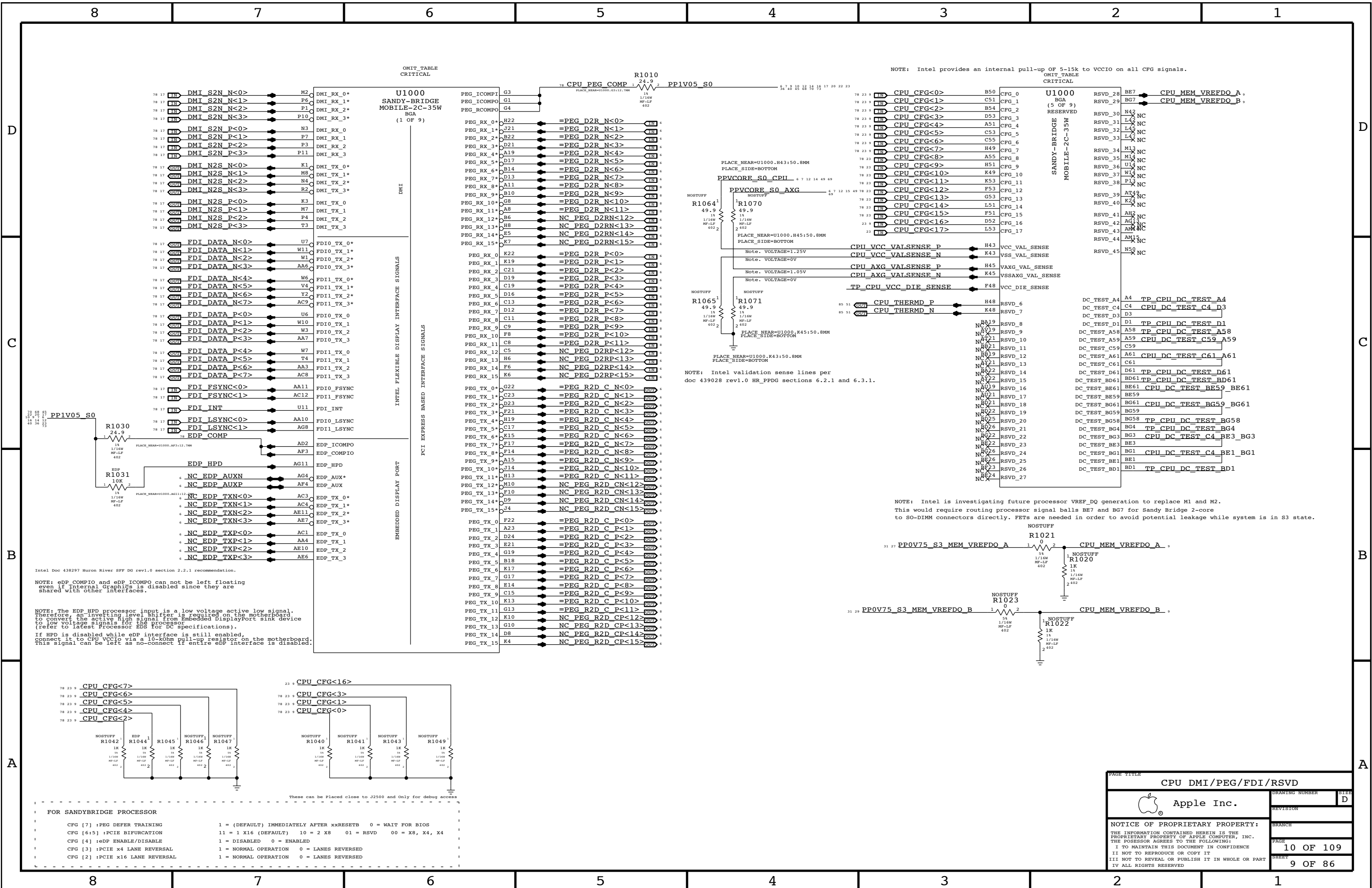
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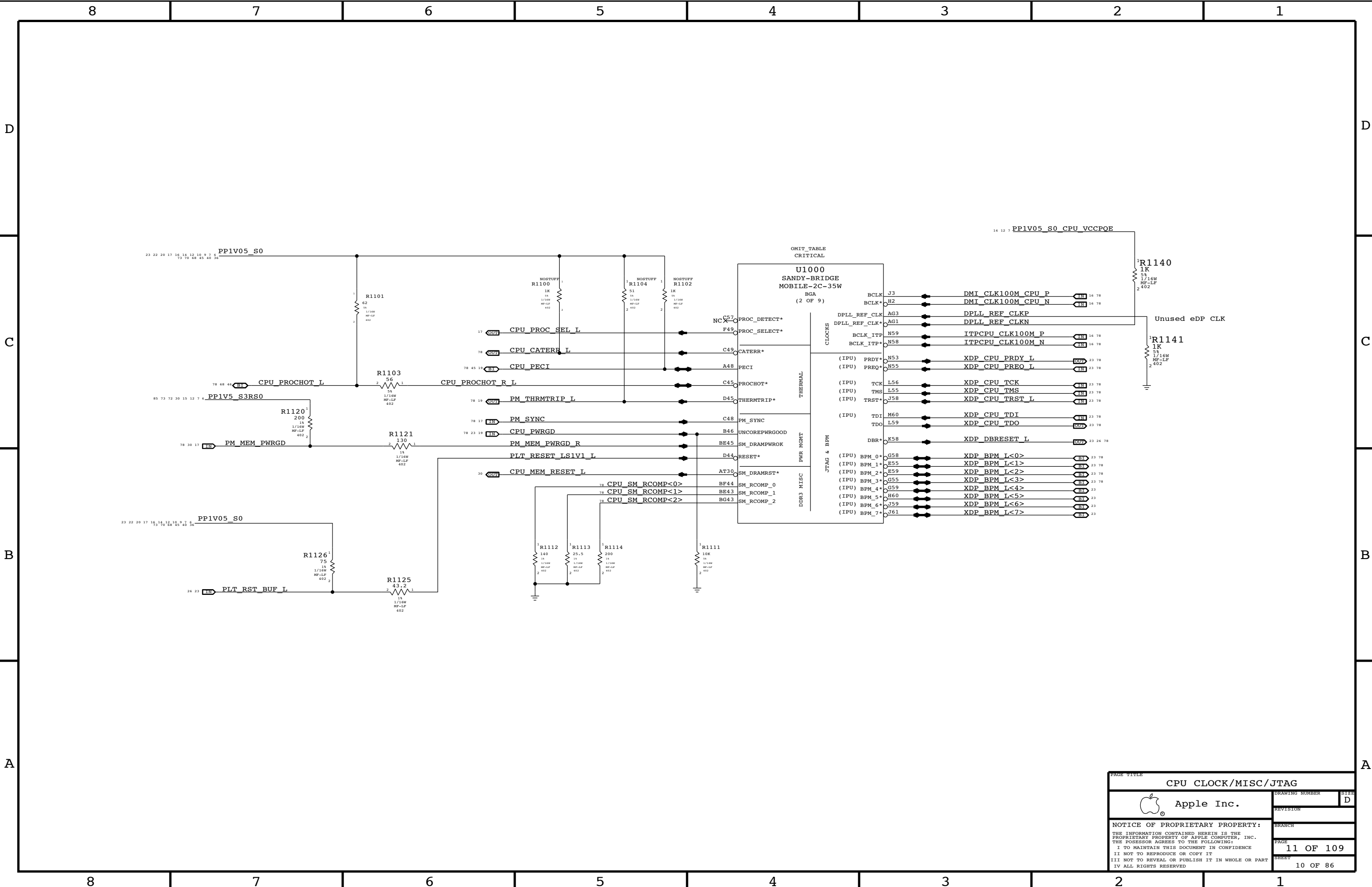
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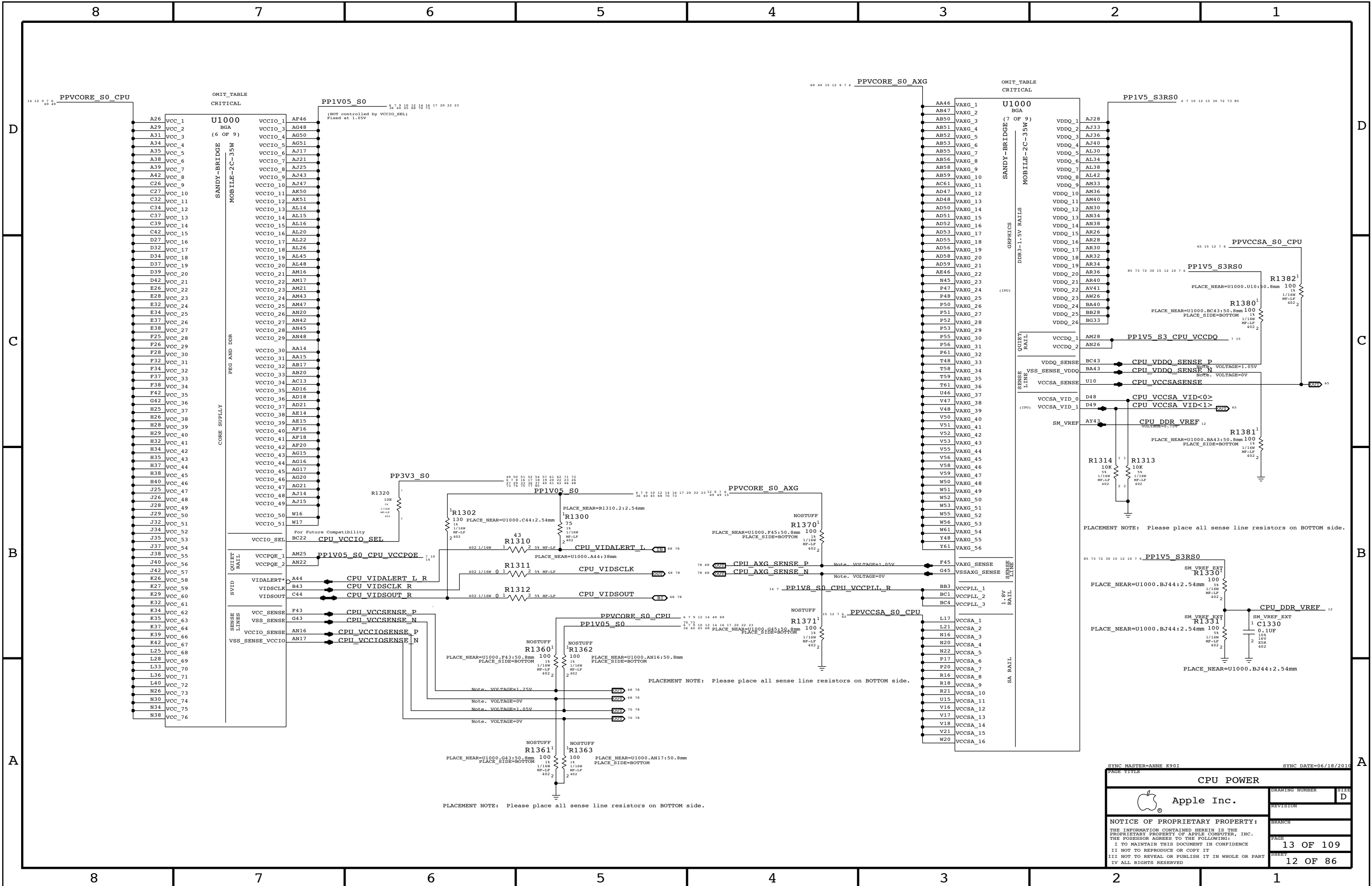
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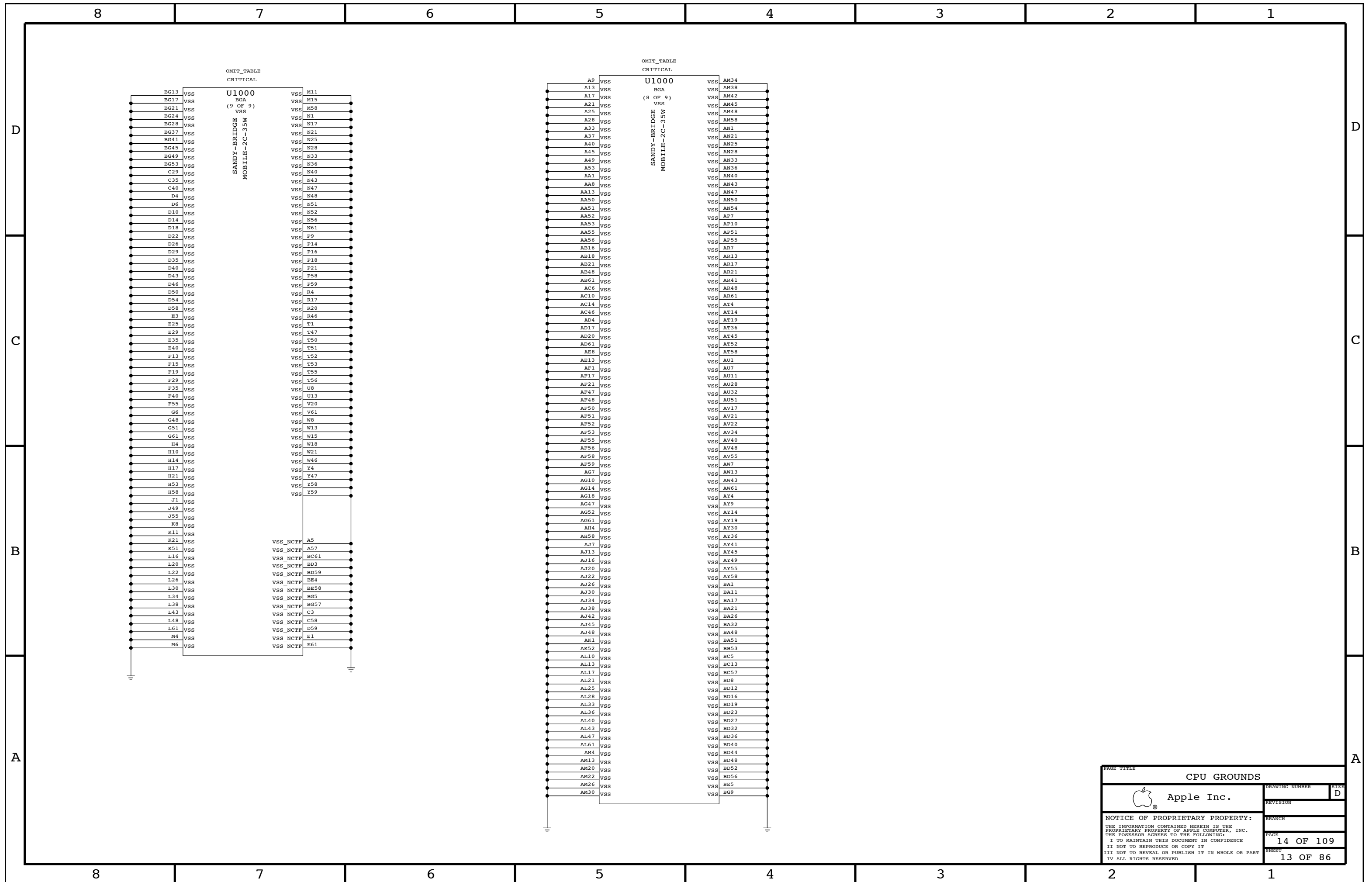


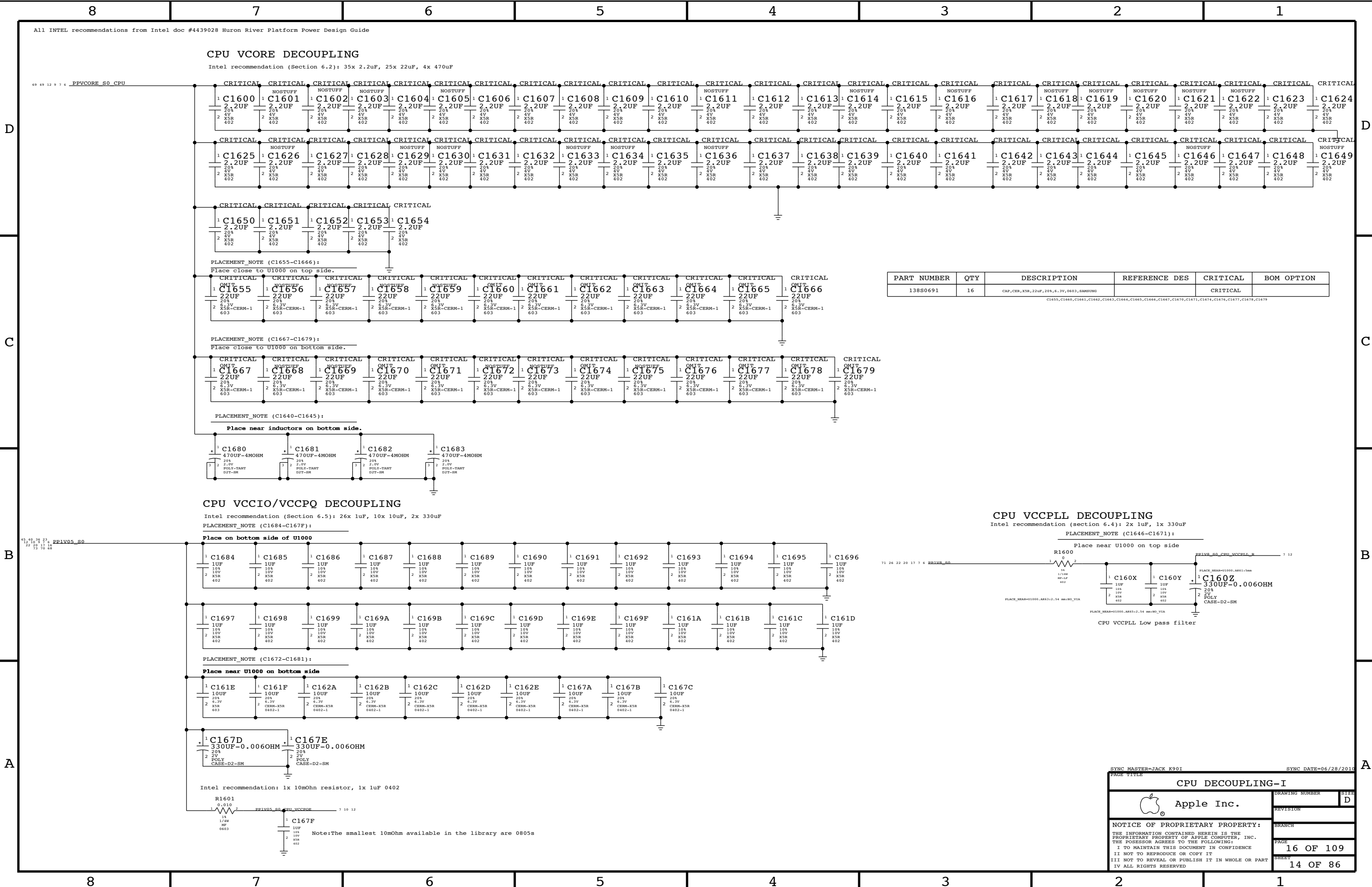




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	SANDY-BRIDGE MOBILE-2C-35W		SANDY-BRIDGE MOBILE-2C-35W		SANDY-BRIDGE MOBILE-2C-35W		
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	MEM A DO<2>		MEM A CKE<0>		MEM B DO<2>		
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	MEM A DO<36>		MEM A BS<2>		MEM B DO<36>		
	MEM A DO<37>		MEM A CAS L		MEM B DO<37>		







C167D

330UF-0.006OHM

20% 2V POLY CASE-D2-SM

C167E

330UF-0.006OHM

20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

R1601

0.010

1% 1/4W NP 0603

C167F

1UF

10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side

R1600

0

5% 1/4W NP-LF 402

C160X

1UF

10% 10V X5R 402

C160Y

1UF

10% 10V X5R 402

C160Z

330UF-0.006OHM

20% 2V POLY CASE-D2-SM

CPU VCCPLL Low pass filter

45 40 36 33 PP1V05_S0

R1601

0.010

1% 1/4W NP 0603

C167F

1UF

10% 10V X5R 402

87654321

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	16	CAP,CER,X5R,22uF,20%,6.3V,0603,SAMSUNG	C1655,C1660,C1661,C1662,C1663,C1664,C1665,C1666,C1667,C1670,C1671,C1674,C1676,C1677,C1678,C1679	CRITICAL	

SYNC MASTER=JACK K90I

SYNC DATE=06/28/2010

CPU DECOUPLING-I

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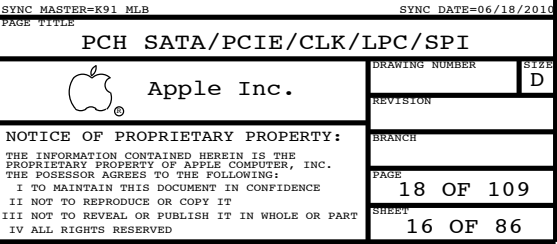
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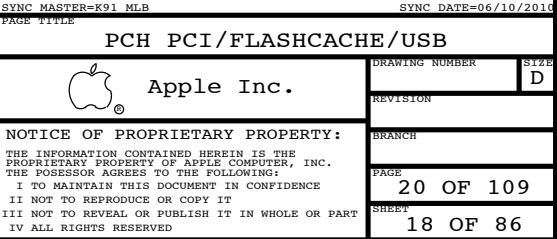
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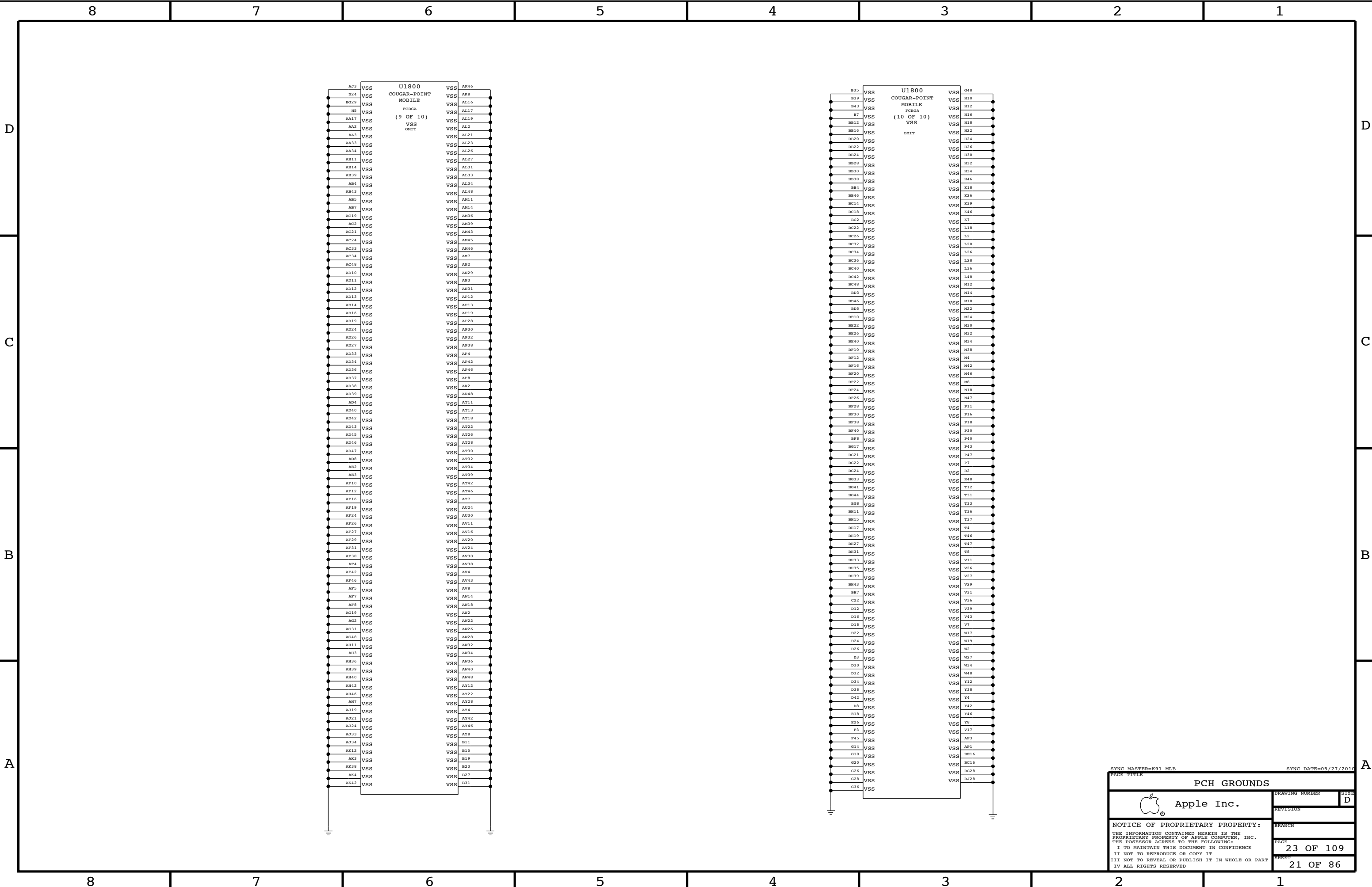
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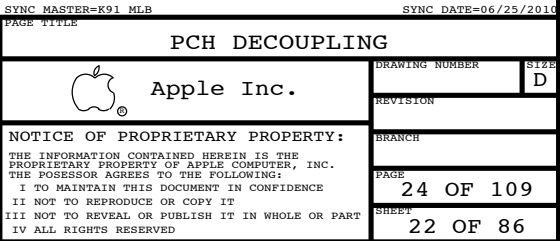
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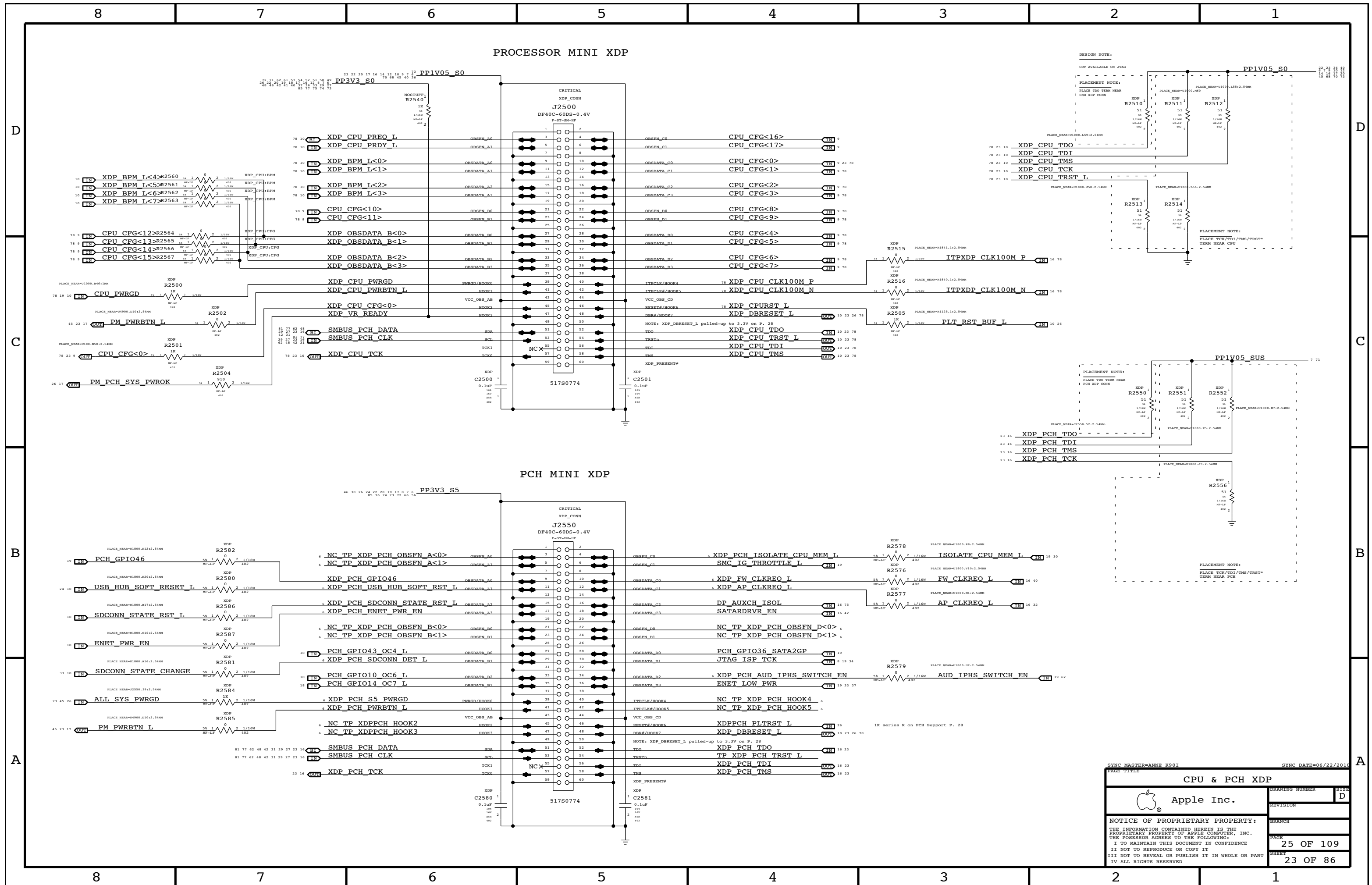
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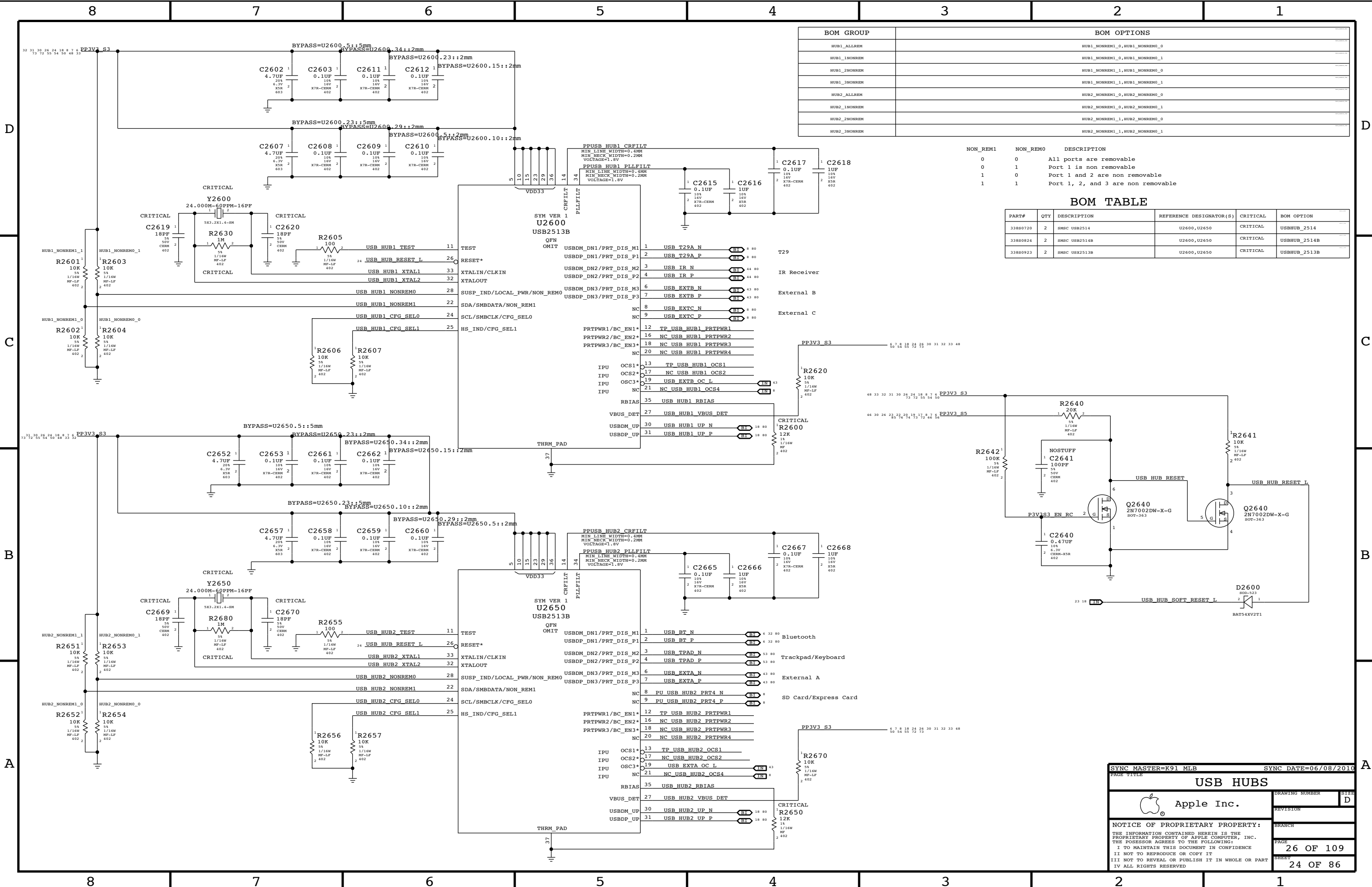












BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREMO_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREMO_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREMO_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREMO_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREMO_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREMO_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREMO_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREMO_1

NON_REM1	NON_REMO	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33850720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
33850824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
33850923	2	SMSC USB2513B	U2600,U2650	CRITICAL	USBHUB_2513B

SYNC MASTER=K91 MLB

SYNC DATE=06/08/2010

PAGE TITLE

USB HUBS

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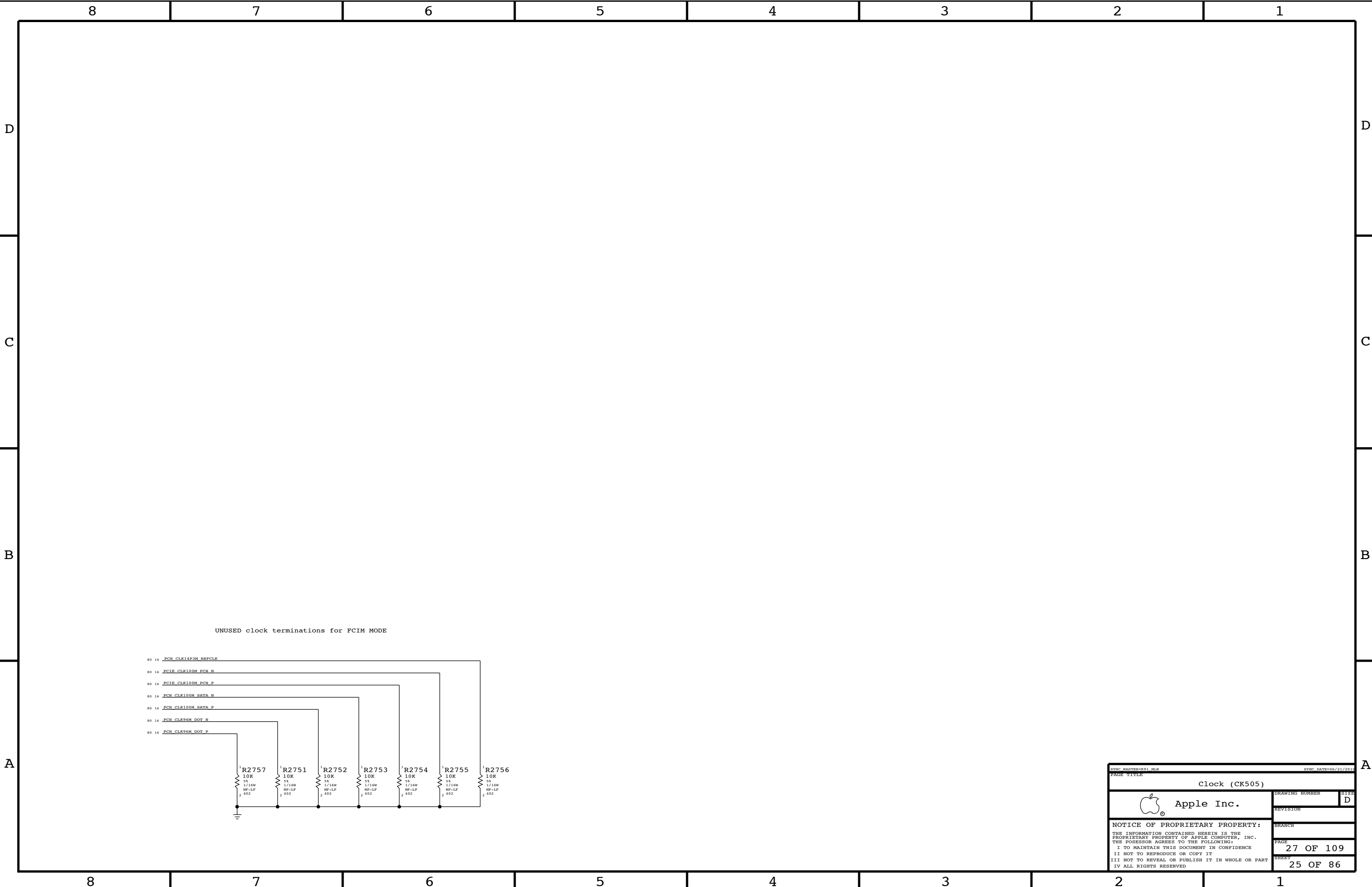
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SYNC MASTER=K1 WEB

SYNC DATE=06/21/2015

PAGE TITLE		Clock (CK505)	
 Apple Inc.		DRAWING NUMBER	SIZE D
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System RTC Power Source & 32kHz / 25MHz Clock Generator

Platform Reset Connections

Unbuffered


Buffered

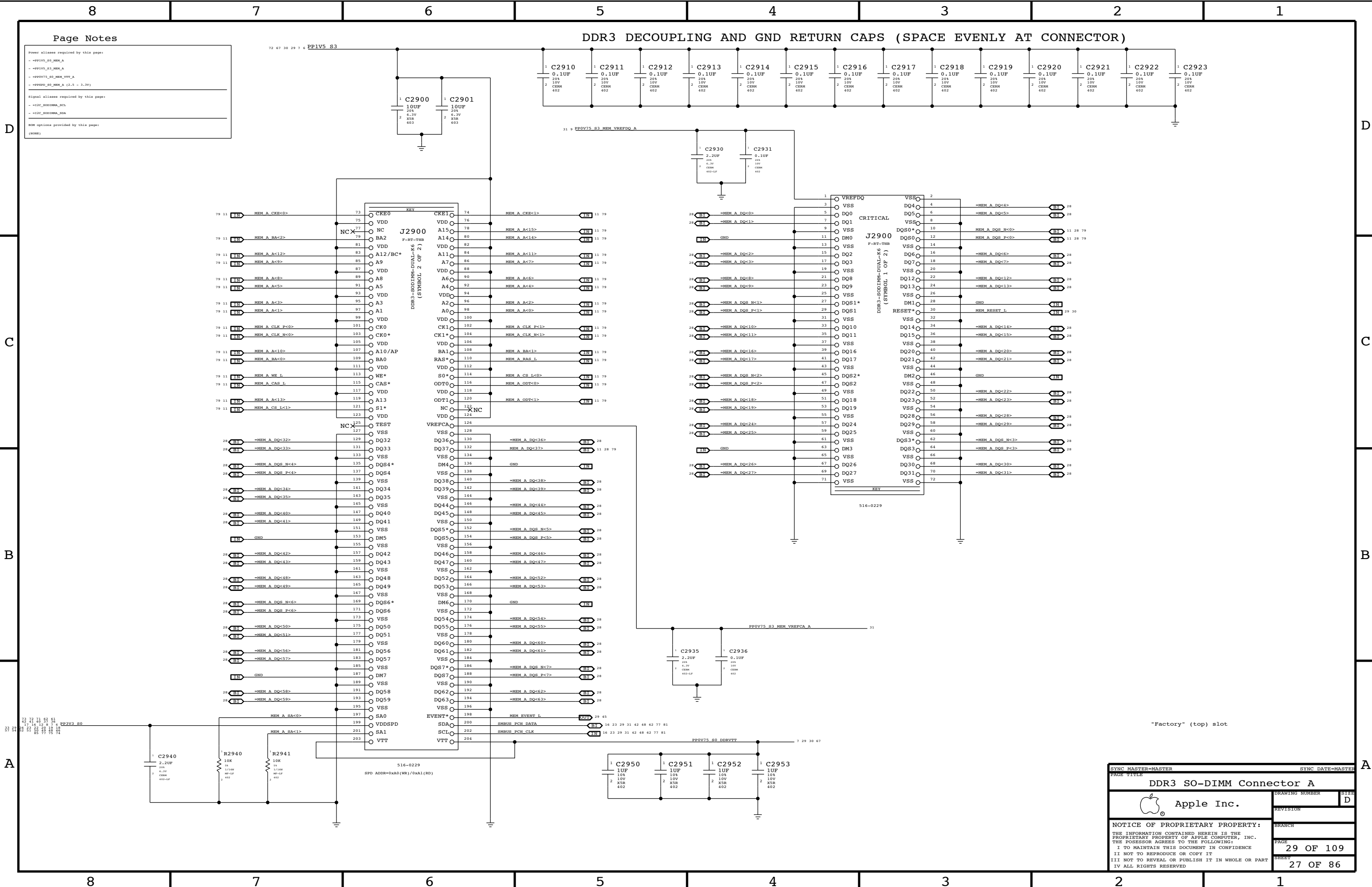
ENET_MEDIA_SENSE ISOLATION CIRCUIT

Ethernet WAKE# Isolation

PCH S0 PWRGD

PCH Reset Button

SYNC MASTER=LINDA K90I		SYNC DATE=07/08/2010	
PAGE TITLE			
Chipset Support			
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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:

- PP1V5_S3_MEM_A
- PP1V5_S3_MEM_A
- PP0V75_S3_MEM_VTT_A
- PPSPD_S3_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- I2C_SODIMM_SCL
- I2C_SODIMM_SDA

DEM options provided by this page:

(NONE)


SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
DDR3 SO-DIMM Connector A			
DRAWING NUMBER		SIZE	
D		D	
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8	7	6	5	4	3	2	1
D	CPU CHANNEL A DQS 0 -> DIMM A DQS 0		CPU CHANNEL B DQS 0 -> DIMM B DQS 0				
	79 28 27 11	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	==	MEM_A_DQS_N<0>	11 27 28 79 79 29 28 11	MEM_B_DQS_N<0>
	79 28 27 11	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	==	MEM_A_DQS_P<0>	11 27 28 79 79 29 28 11	MEM_B_DQS_P<0>
				==	GND		
	79 11	MEM_A_DQ<7>	MAKE_BASE=TRUE	==	MEM_A_DQ<3>	27	
	79 11	MEM_A_DQ<6>	MAKE_BASE=TRUE	==	MEM_A_DQ<6>	27	
	79 11	MEM_A_DQ<5>	MAKE_BASE=TRUE	==	MEM_A_DQ<1>	27	
	79 11	MEM_A_DQ<4>	MAKE_BASE=TRUE	==	MEM_A_DQ<5>	27	
	79 11	MEM_A_DQ<3>	MAKE_BASE=TRUE	==	MEM_A_DQ<2>	27	
	79 11	MEM_A_DQ<2>	MAKE_BASE=TRUE	==	MEM_A_DQ<7>	27	
	79 11	MEM_A_DQ<1>	MAKE_BASE=TRUE	==	MEM_A_DQ<0>	27	
	79 11	MEM_A_DQ<0>	MAKE_BASE=TRUE	==	MEM_A_DQ<4>	27	
				==	GND		
	79 11	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	==	MEM_A_DQS_N<1>	27	
	79 11	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	==	MEM_A_DQS_P<1>	27	
				==	GND		
	79 11	MEM_A_DQ<15>	MAKE_BASE=TRUE	==	MEM_A_DQ<11>	27	
	79 11	MEM_A_DQ<14>	MAKE_BASE=TRUE	==	MEM_A_DQ<10>	27	
	79 11	MEM_A_DQ<13>	MAKE_BASE=TRUE	==	MEM_A_DQ<12>	27	
	79 11	MEM_A_DQ<12>	MAKE_BASE=TRUE	==	MEM_A_DQ<9>	27	
	79 11	MEM_A_DQ<11>	MAKE_BASE=TRUE	==	MEM_A_DQ<15>	27	
	79 11	MEM_A_DQ<10>	MAKE_BASE=TRUE	==	MEM_A_DQ<14>	27	
	79 11	MEM_A_DQ<9>	MAKE_BASE=TRUE	==	MEM_A_DQ<13>	27	
	79 11	MEM_A_DQ<8>	MAKE_BASE=TRUE	==	MEM_A_DQ<8>	27	
				==	GND		
	79 11	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	==	MEM_A_DQS_N<2>	27	
	79 11	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	==	MEM_A_DQS_P<2>	27	
				==	GND		
	79 11	MEM_A_DQ<23>	MAKE_BASE=TRUE	==	MEM_A_DQ<23>	27	
	79 11	MEM_A_DQ<22>	MAKE_BASE=TRUE	==	MEM_A_DQ<22>	27	
	79 11	MEM_A_DQ<21>	MAKE_BASE=TRUE	==	MEM_A_DQ<21>	27	
	79 11	MEM_A_DQ<20>	MAKE_BASE=TRUE	==	MEM_A_DQ<20>	27	
	79 11	MEM_A_DQ<19>	MAKE_BASE=TRUE	==	MEM_A_DQ<18>	27	
	79 11	MEM_A_DQ<18>	MAKE_BASE=TRUE	==	MEM_A_DQ<19>	27	
	79 11	MEM_A_DQ<17>	MAKE_BASE=TRUE	==	MEM_A_DQ<16>	27	
	79 11	MEM_A_DQ<16>	MAKE_BASE=TRUE	==	MEM_A_DQ<17>	27	
C	CPU CHANNEL A DQS 3 -> DIMM A DQS 3		CPU CHANNEL B DQS 3 -> DIMM B DQS 3				
	79 11	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	==	MEM_A_DQS_N<3>	27	
	79 11	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	==	MEM_A_DQS_P<3>	27	
				==	GND		
	79 11	MEM_A_DQ<31>	MAKE_BASE=TRUE	==	MEM_A_DQ<26>	27	
	79 11	MEM_A_DQ<30>	MAKE_BASE=TRUE	==	MEM_A_DQ<24>	27	
	79 11	MEM_A_DQ<29>	MAKE_BASE=TRUE	==	MEM_A_DQ<28>	27	
	79 11	MEM_A_DQ<28>	MAKE_BASE=TRUE	==	MEM_A_DQ<25>	27	
	79 11	MEM_A_DQ<27>	MAKE_BASE=TRUE	==	MEM_A_DQ<31>	27	
	79 11	MEM_A_DQ<26>	MAKE_BASE=TRUE	==	MEM_A_DQ<27>	27	
	79 11	MEM_A_DQ<25>	MAKE_BASE=TRUE	==	MEM_A_DQ<30>	27	
	79 11	MEM_A_DQ<24>	MAKE_BASE=TRUE	==	MEM_A_DQ<29>	27	
				==	GND		
	79 11	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	==	MEM_A_DQS_N<4>	27	
	79 11	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	==	MEM_A_DQS_P<4>	27	
				==	GND		
	79 11	MEM_A_DQ<39>	MAKE_BASE=TRUE	==	MEM_A_DQ<38>	27	
	79 11	MEM_A_DQ<38>	MAKE_BASE=TRUE	==	MEM_A_DQ<39>	27	
	79 28 27 11	MEM_A_DQ<37>	MAKE_BASE=TRUE	==	MEM_A_DQ<37>	11 27 28 79 79 29 28 11	MEM_B_DQ<37>
	79 11	MEM_A_DQ<36>	MAKE_BASE=TRUE	==	MEM_A_DQ<33>	27	
	79 11	MEM_A_DQ<35>	MAKE_BASE=TRUE	==	MEM_A_DQ<34>	27	
	79 11	MEM_A_DQ<34>	MAKE_BASE=TRUE	==	MEM_A_DQ<35>	27	
	79 11	MEM_A_DQ<33>	MAKE_BASE=TRUE	==	MEM_A_DQ<32>	27	
	79 11	MEM_A_DQ<32>	MAKE_BASE=TRUE	==	MEM_A_DQ<36>	27	
B	CPU CHANNEL A DQS 5 -> DIMM A DQS 5		CPU CHANNEL B DQS 5 -> DIMM B DQS 5				
	79 11	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	==	MEM_A_DQS_N<5>	27	
	79 11	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	==	MEM_A_DQS_P<5>	27	
				==	GND		
	79 11	MEM_A_DQ<47>	MAKE_BASE=TRUE	==	MEM_A_DQ<46>	27	
	79 11	MEM_A_DQ<46>	MAKE_BASE=TRUE	==	MEM_A_DQ<43>	27	
	79 11	MEM_A_DQ<45>	MAKE_BASE=TRUE	==	MEM_A_DQ<45>	27	
	79 11	MEM_A_DQ<44>	MAKE_BASE=TRUE	==	MEM_A_DQ<41>	27	
	79 11	MEM_A_DQ<43>	MAKE_BASE=TRUE	==	MEM_A_DQ<47>	27	
	79 11	MEM_A_DQ<42>	MAKE_BASE=TRUE	==	MEM_A_DQ<42>	27	
	79 11	MEM_A_DQ<41>	MAKE_BASE=TRUE	==	MEM_A_DQ<40>	27	
	79 11	MEM_A_DQ<40>	MAKE_BASE=TRUE	==	MEM_A_DQ<44>	27	
				==	GND		
	79 11	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	==	MEM_A_DQS_N<6>	27	
	79 11	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	==	MEM_A_DQS_P<6>	27	
				==	GND		
	79 11	MEM_A_DQ<55>	MAKE_BASE=TRUE	==	MEM_A_DQ<51>	27	
	79 11	MEM_A_DQ<54>	MAKE_BASE=TRUE	==	MEM_A_DQ<54>	27	
	79 11	MEM_A_DQ<53>	MAKE_BASE=TRUE	==	MEM_A_DQ<49>	27	
	79 11	MEM_A_DQ<52>	MAKE_BASE=TRUE	==	MEM_A_DQ<53>	27	
	79 11	MEM_A_DQ<51>	MAKE_BASE=TRUE	==	MEM_A_DQ<50>	27	
	79 11	MEM_A_DQ<50>	MAKE_BASE=TRUE	==	MEM_A_DQ<55>	27	
	79 11	MEM_A_DQ<49>	MAKE_BASE=TRUE	==	MEM_A_DQ<48>	27	
	79 11	MEM_A_DQ<48>	MAKE_BASE=TRUE	==	MEM_A_DQ<52>	27	
A	CPU CHANNEL A DQS 7 -> DIMM A DQS 7		CPU CHANNEL B DQS 7 -> DIMM B DQS 7				
	79 11	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	==	MEM_A_DQS_N<7>	27	
	79 11	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	==	MEM_A_DQS_P<7>	27	
				==	GND		
	79 11	MEM_A_DQ<63>	MAKE_BASE=TRUE	==	MEM_A_DQ<58>	27	
	79 11	MEM_A_DQ<62>	MAKE_BASE=TRUE	==	MEM_A_DQ<59>	27	
	79 11	MEM_A_DQ<61>	MAKE_BASE=TRUE	==	MEM_A_DQ<60>	27	
	79 11	MEM_A_DQ<60>	MAKE_BASE=TRUE	==	MEM_A_DQ<57>	27	
	79 11	MEM_A_DQ<59>	MAKE_BASE=TRUE	==	MEM_A_DQ<63>	27	
	79 11	MEM_A_DQ<58>	MAKE_BASE=TRUE	==	MEM_A_DQ<62>	27	
	79 11	MEM_A_DQ<57>	MAKE_BASE=TRUE	==	MEM_A_DQ<61>	27	
	79 11	MEM_A_DQ<56>	MAKE_BASE=TRUE	==	MEM_A_DQ<56>	27	
NOTE: Sandybridge does not use DM signals per doc 438297 Huron River SFF DG rev1.0 Section 2.6.13							
8	7	6	5	4	3	2	1

SYNC MASTER=ANNE K901

SYNC DATE=06/22/2010

DDR3 Byte/Bit Swaps



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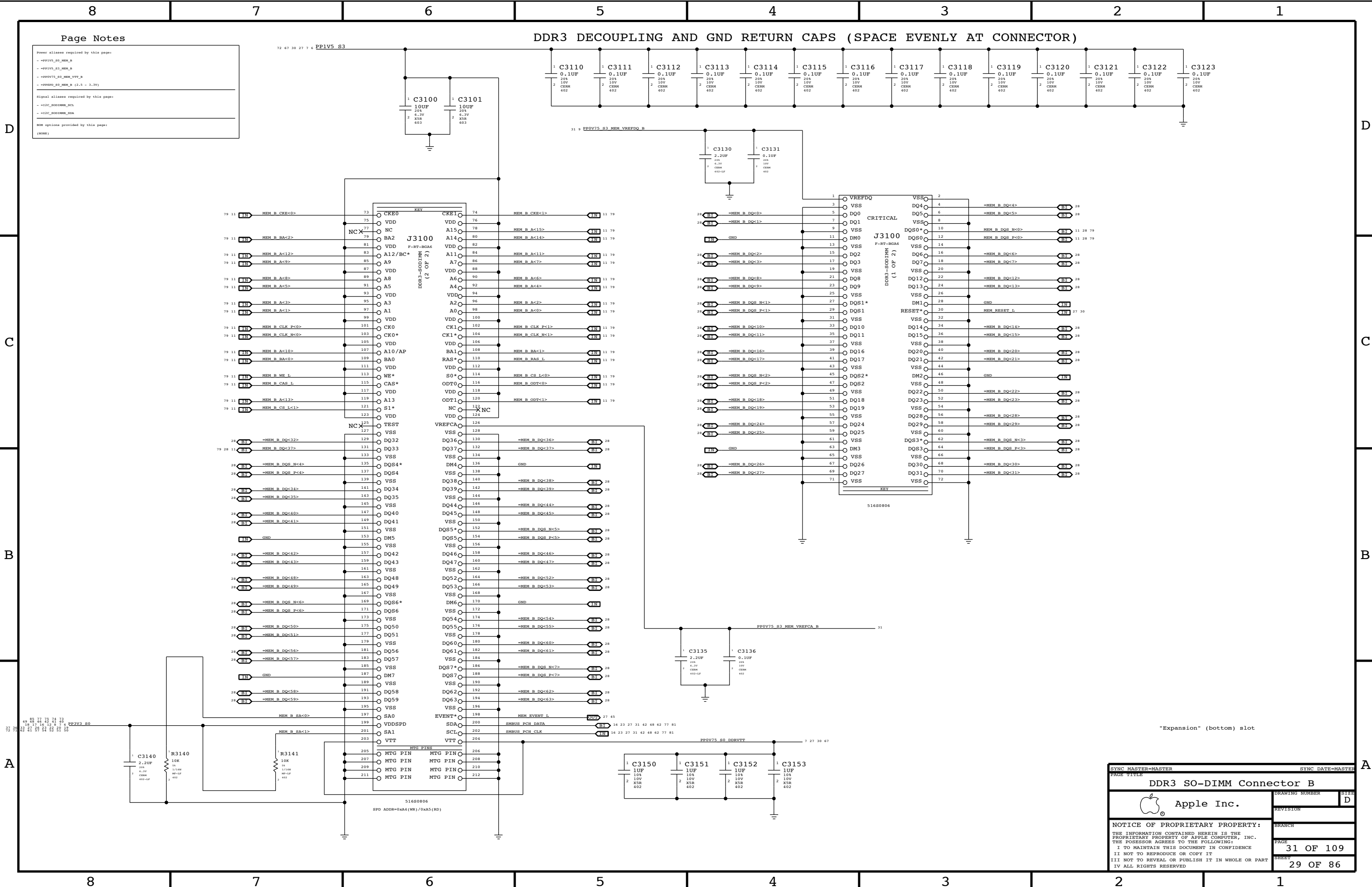
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SIZE

D



Page Notes

Power aliases required by this page:

- PPIV5_S0_MEM_B
- PPIV5_S0_MEM_B
- PPIV5_S0_MEM_VTT_B
- PPIV5_S0_MEM_VTT_B
- PPIV5_S0_MEM_VTT_B

Signal aliases required by this page:

- I2C_S0D1MEM_SCL
- I2C_S0D1MEM_SDA

ROM options provided by this page:

(None)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

"Expansion" (bottom) slot

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
DDR3 SO-DIMM Connector B			
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

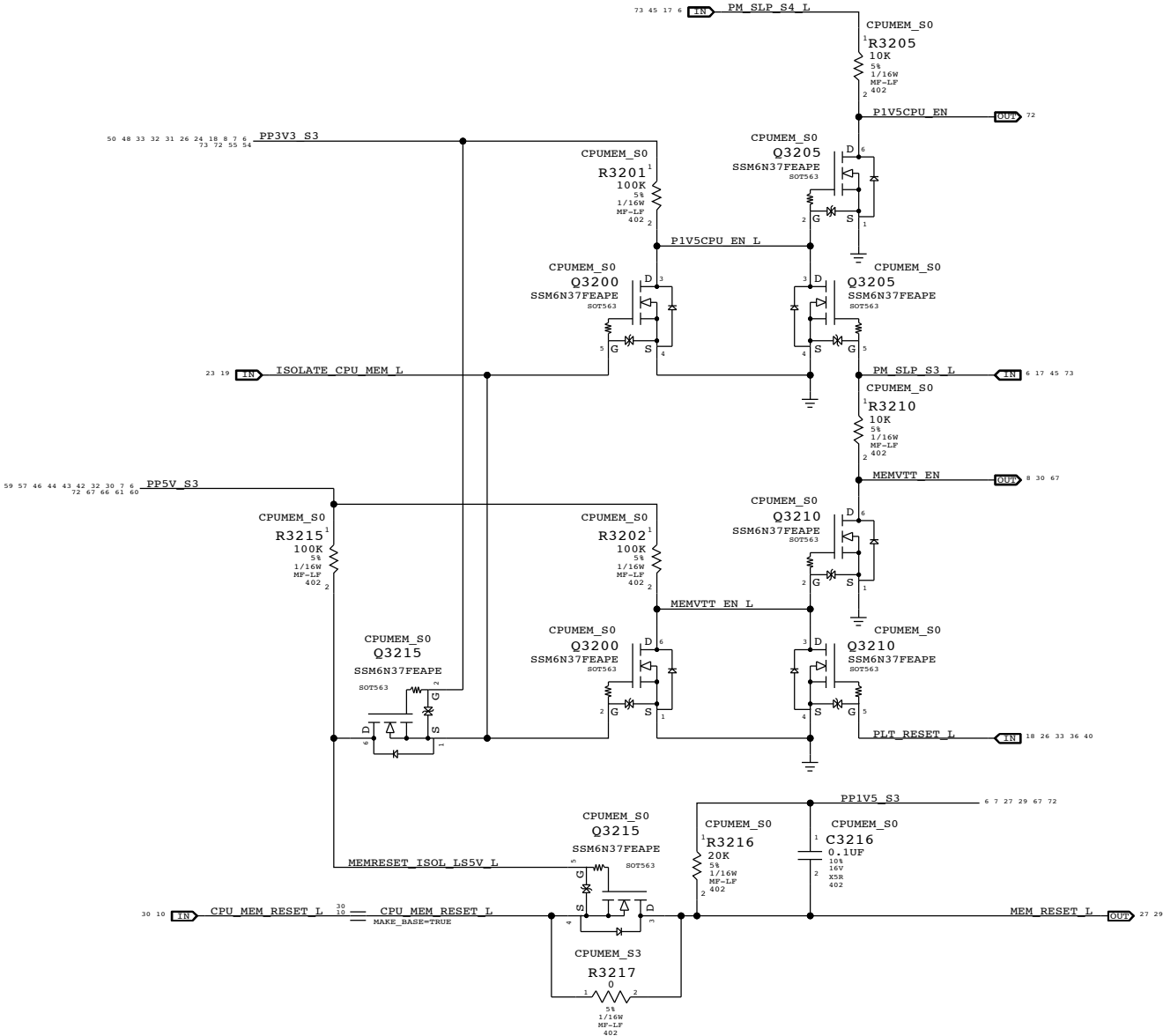
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

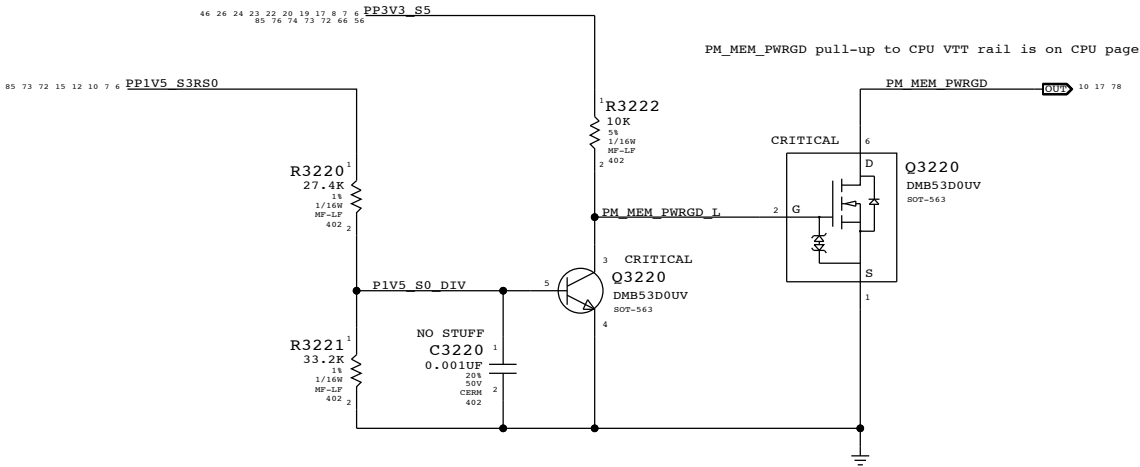
PIV5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

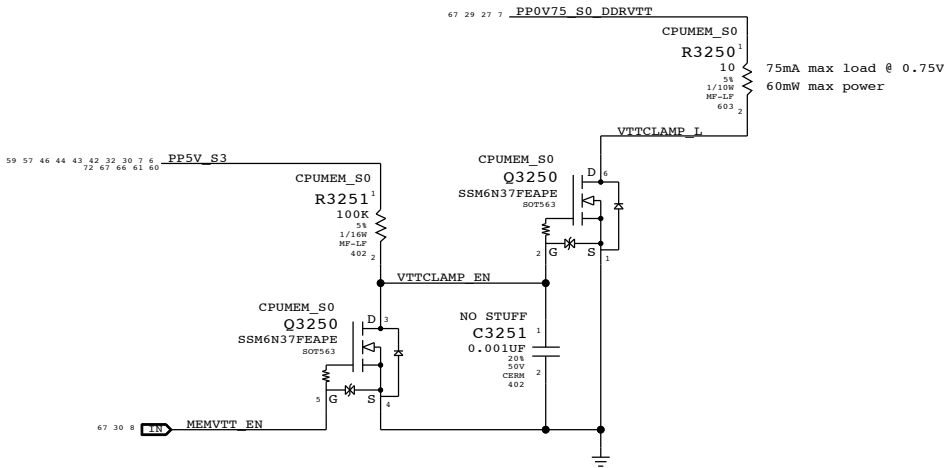


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp


Ensures CKE signals are held low in S3

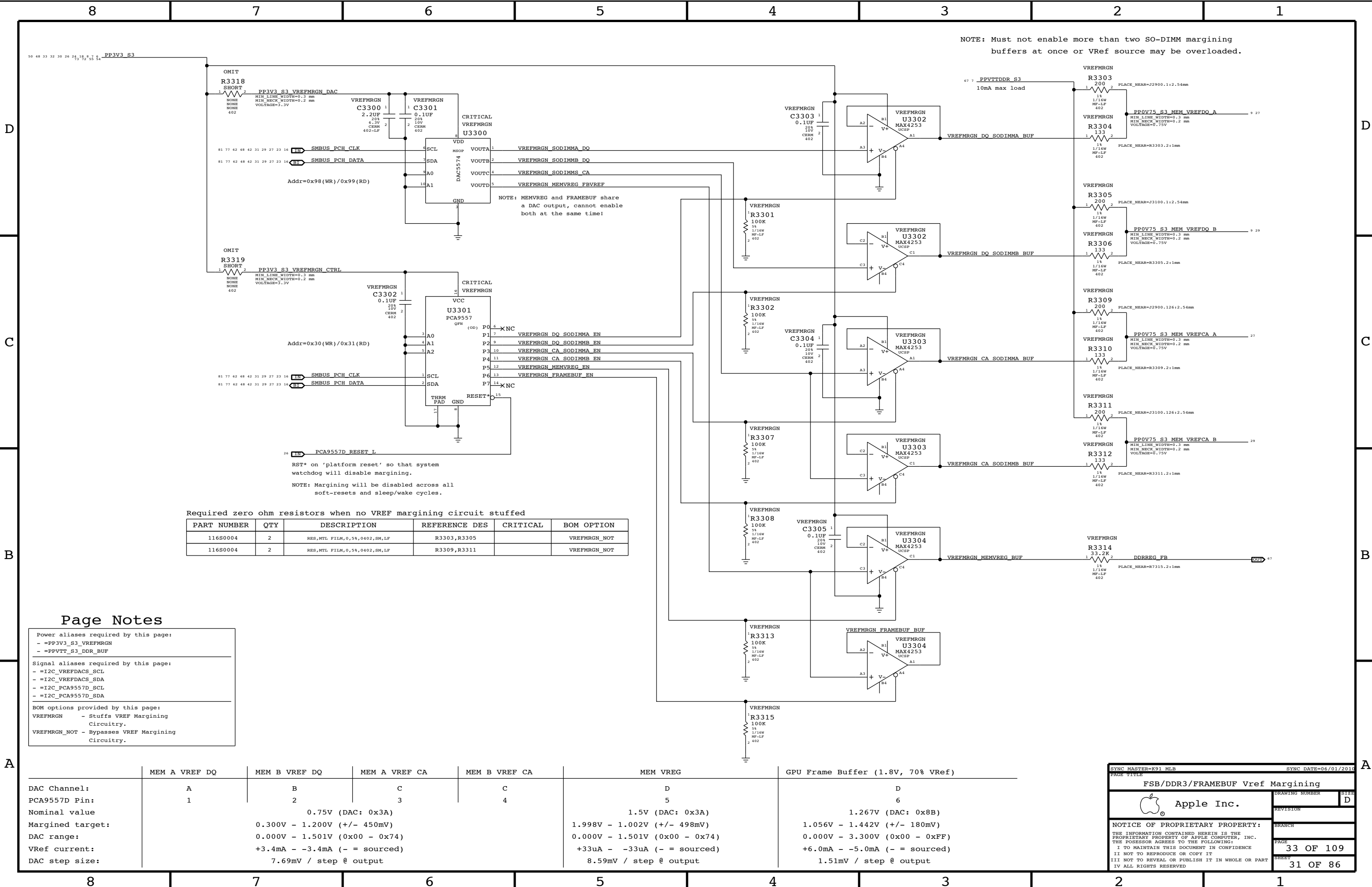


Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	PIV5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=ANNE K901		SYNC DATE=06/22/2010	
PAGE TITLE			
CPU Memory S3 Support			
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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=F91 MELB

SYNC DATE=06/01/2010

FSB/DDR3/FRAMEBUF Vref Margining

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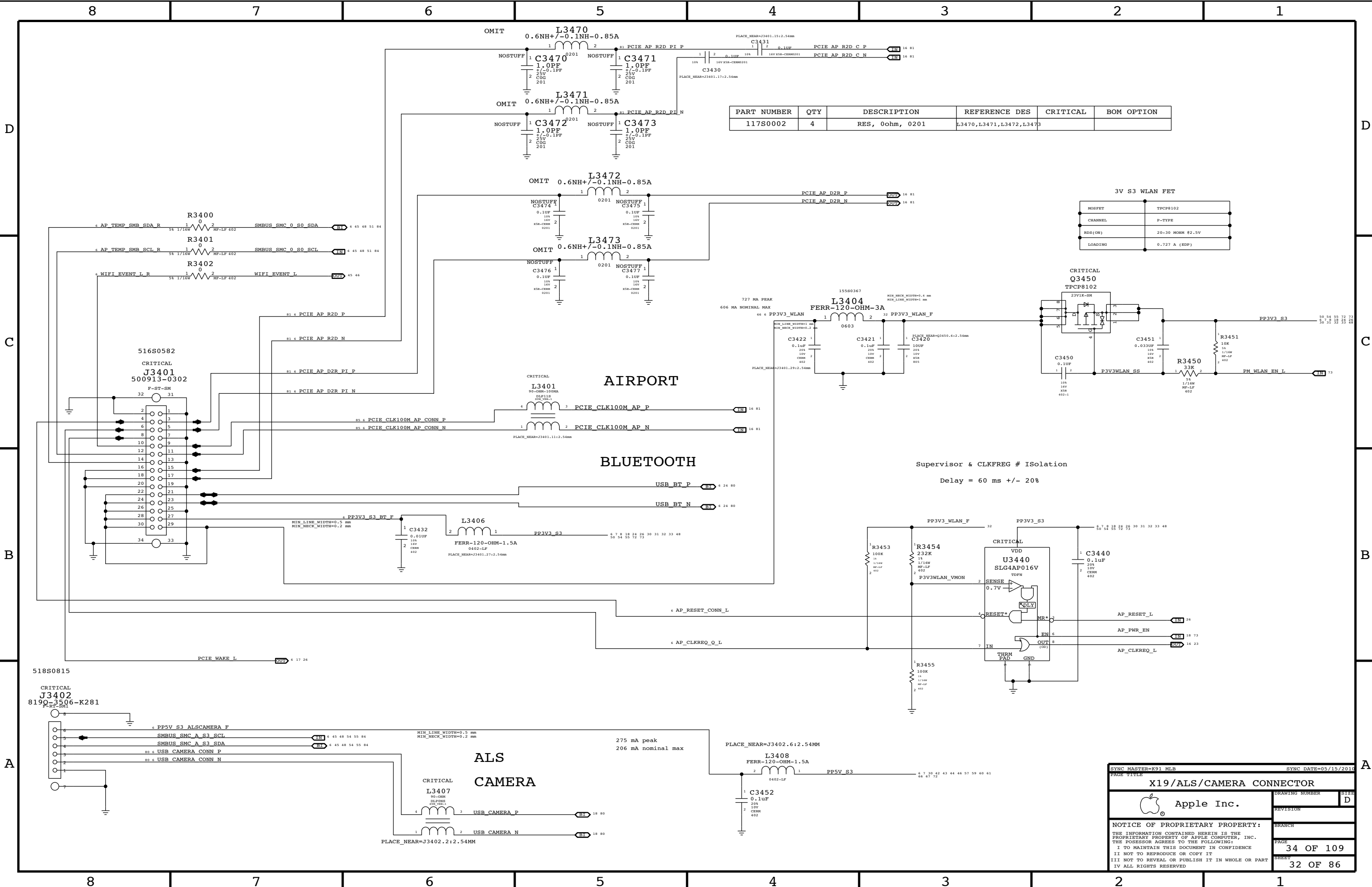
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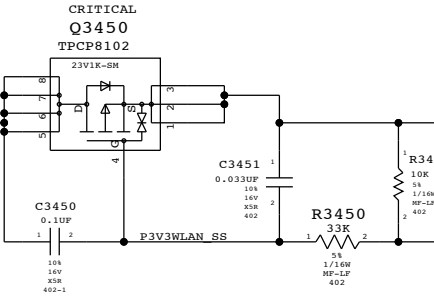
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0ohm, 0201	L3470,L3471,L3472,L3473		


3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.727 A (RDP)



AIRPORT

BLUETOOTH

Supervisor & CLKFREQ # Isolation
Delay = 60 ms +/- 20%

SYNC MASTER=K91 MLB		SYNC DATE=05/15/2010	
PAGE TITLE			
X19/ALS/CAMERA CONNECTOR			
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		PAGE	34 OF 109
		SHEET	32 OF 86

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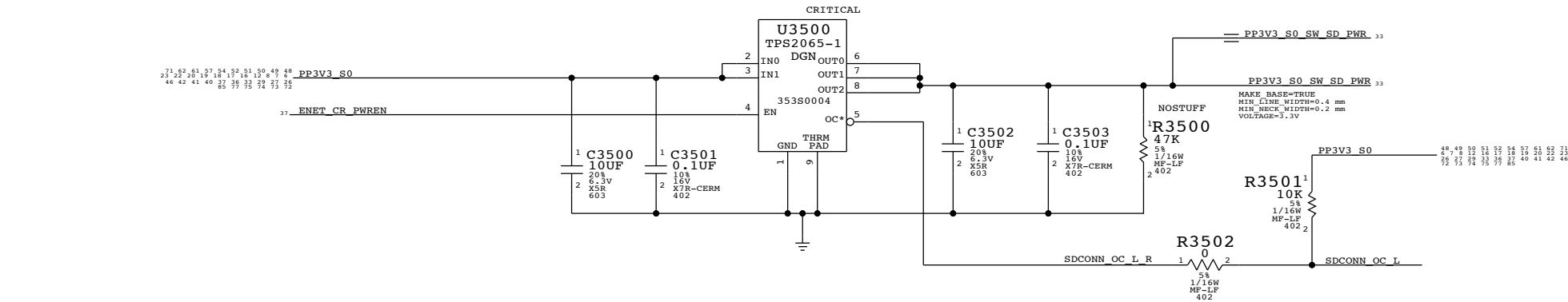
C

B

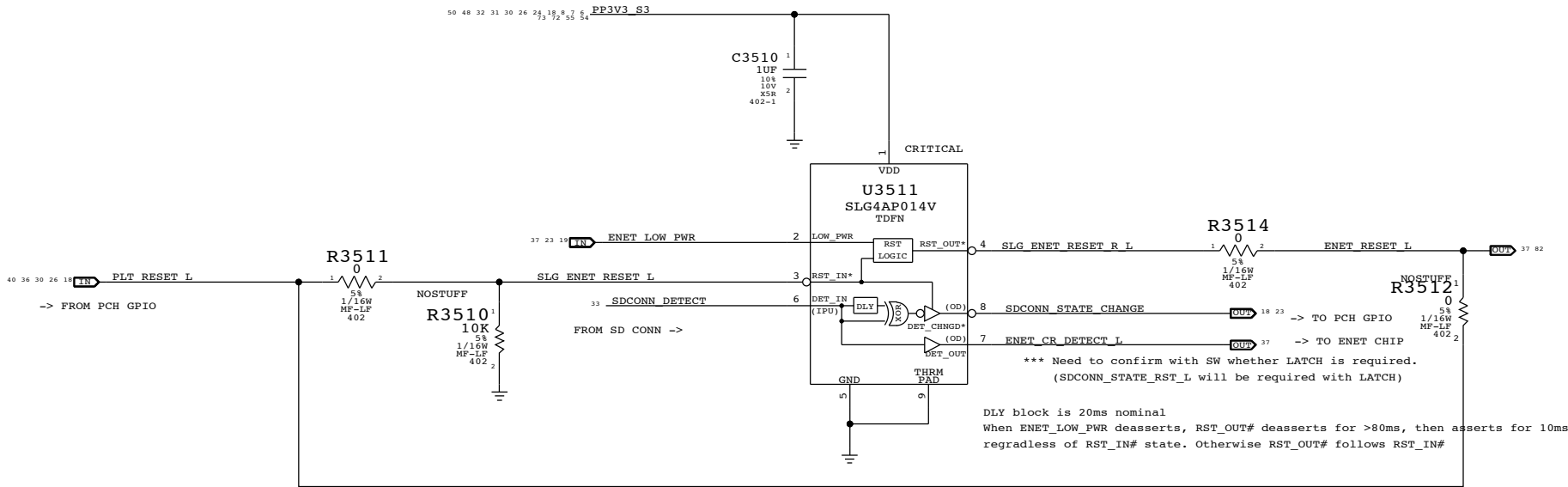
A

SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

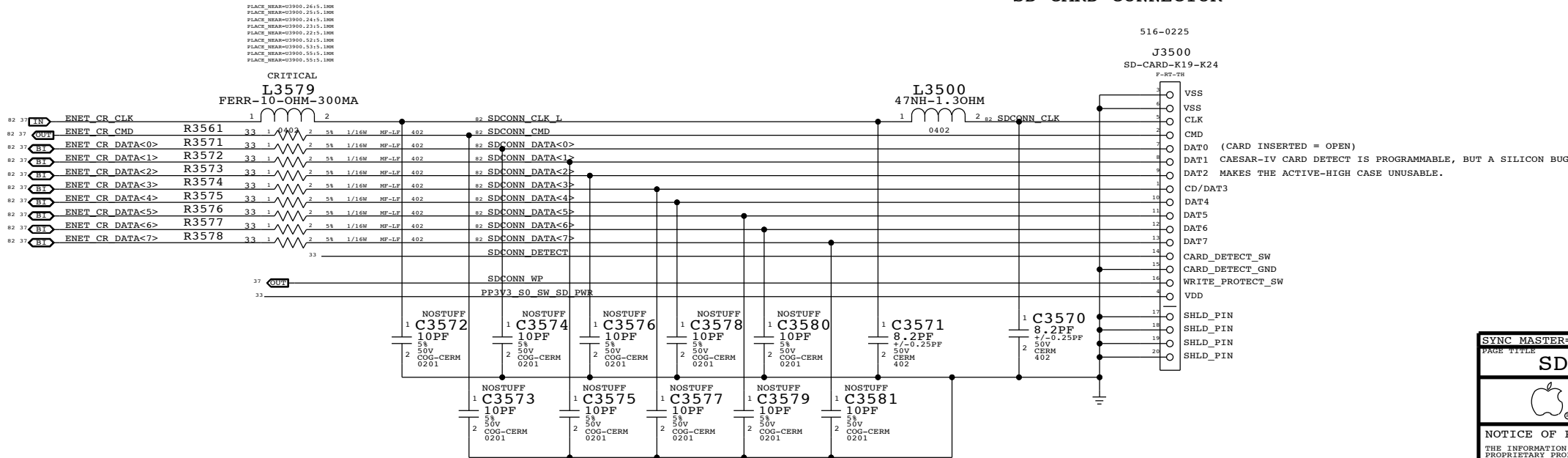
TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



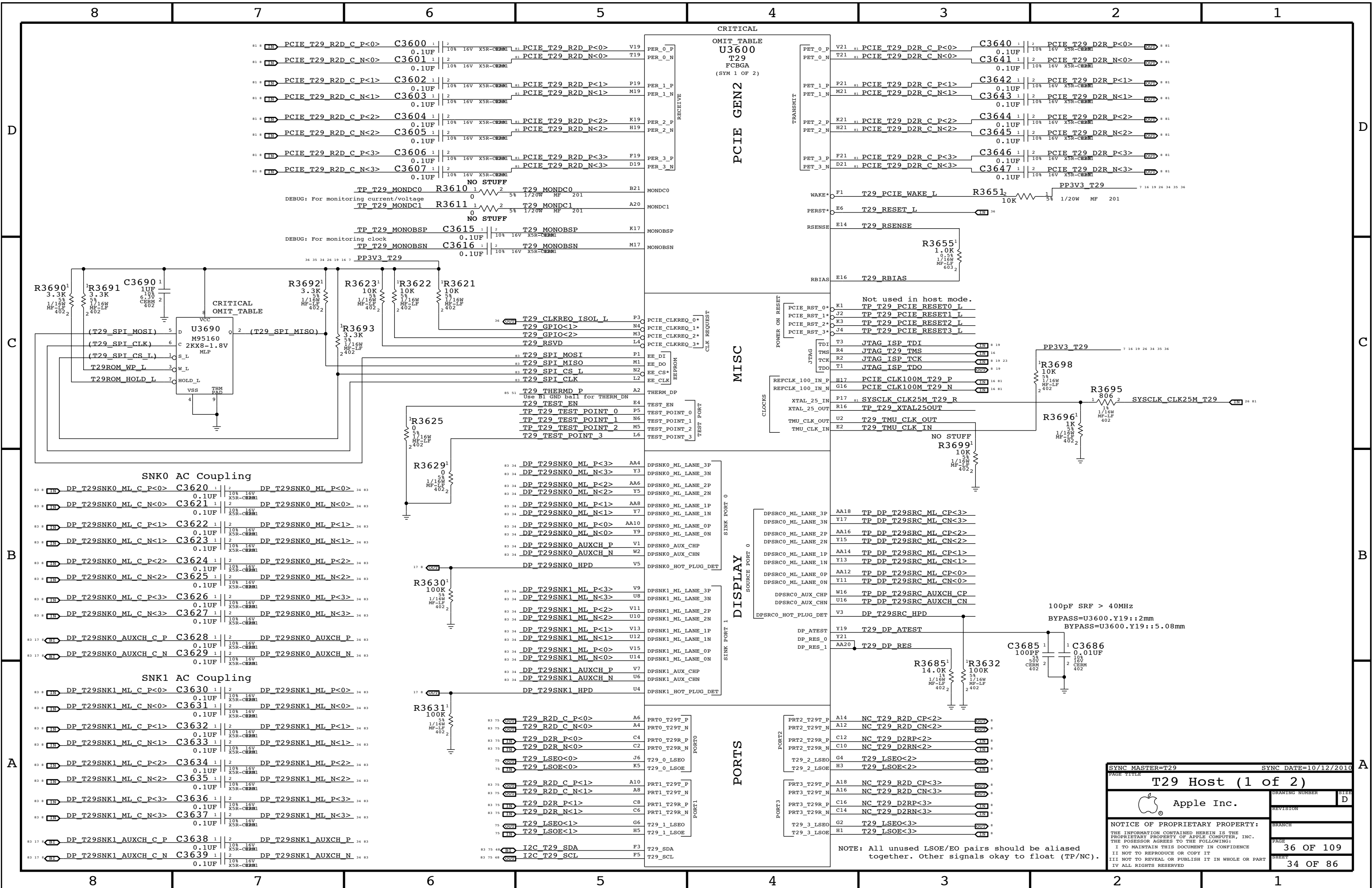
SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SD CARD CONNECTOR



SYNC MASTER=K91 MLB		SYNC DATE=05/26/2010	
PAGE TITLE		SD READER CONNECTOR	
Apple Inc.		DRAWING NUMBER	SIZE D
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8	7	6	5	4	3	2	1
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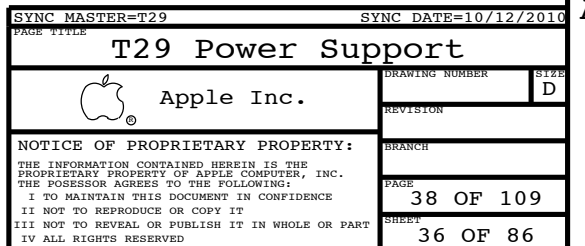
8	7	6	5	4	3	2	1
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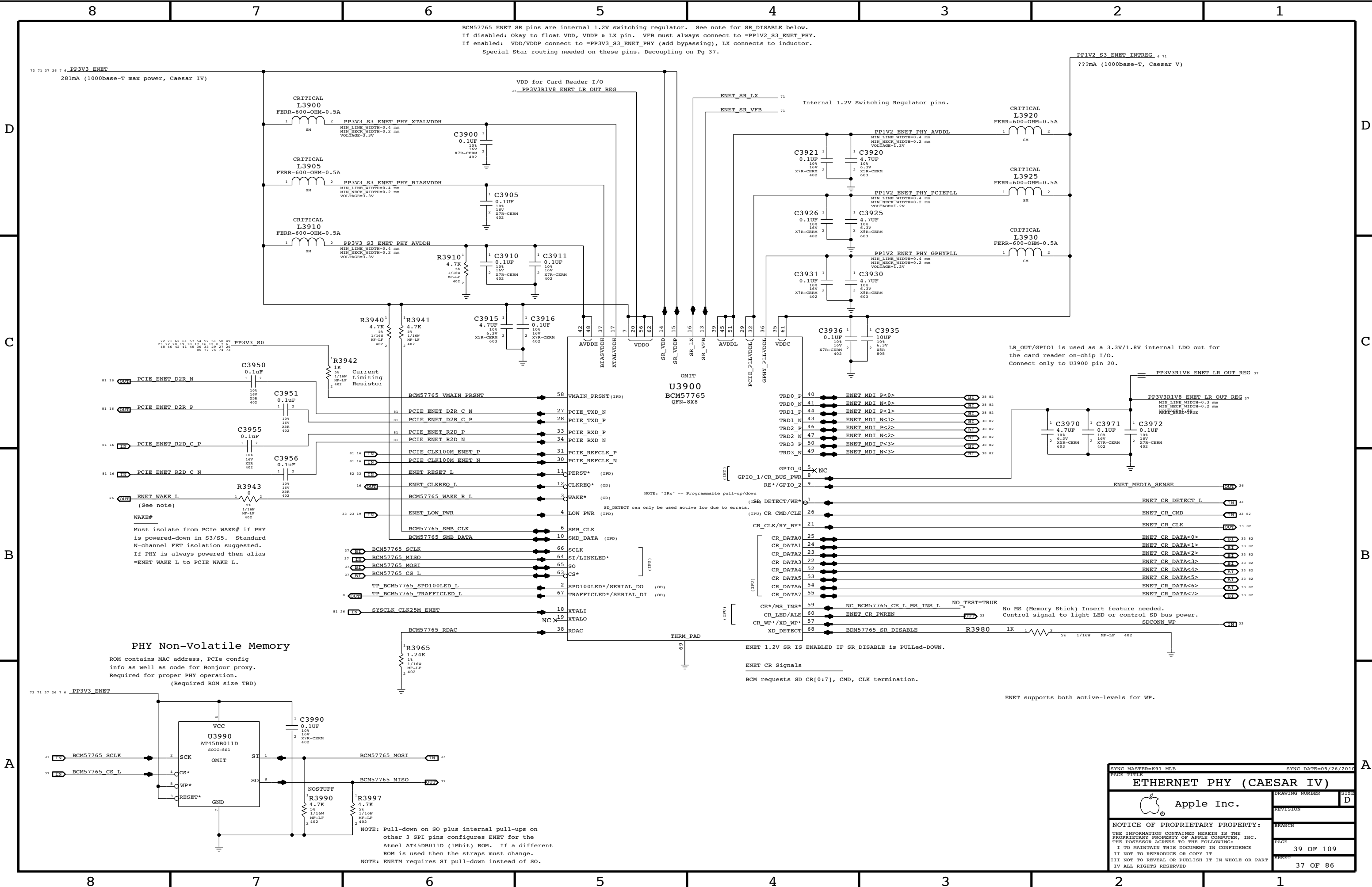


C



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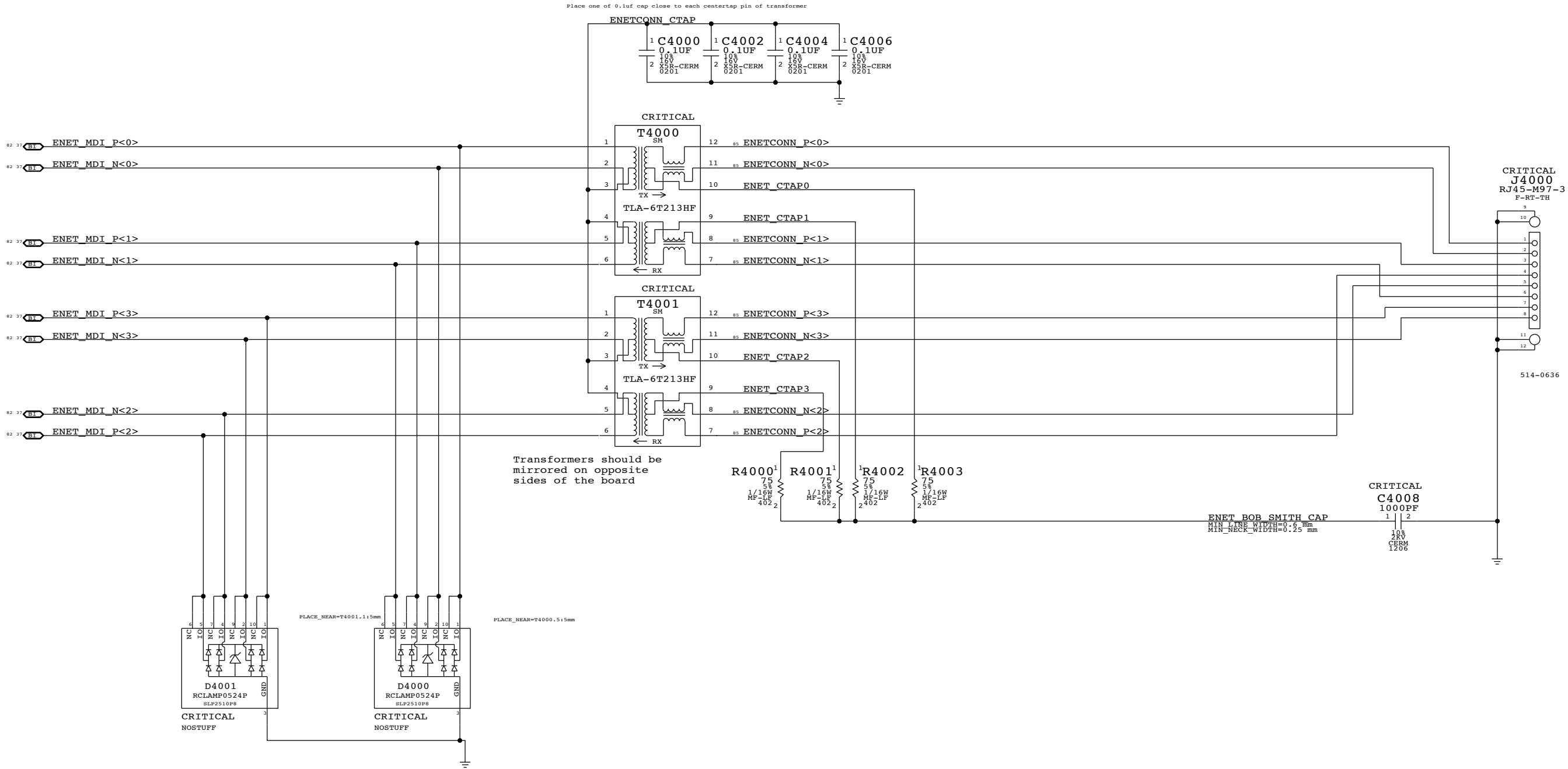



Page Notes

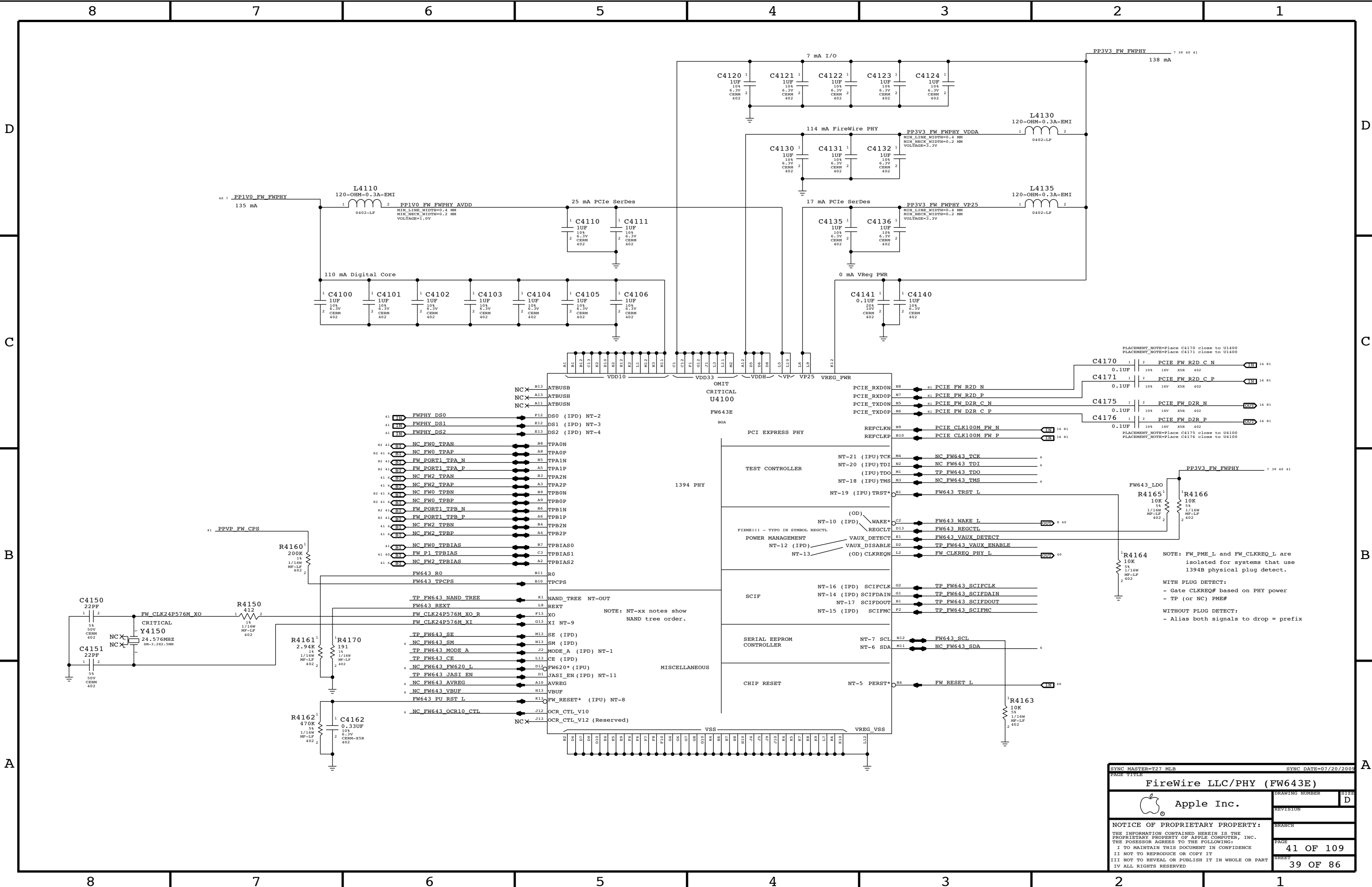
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K91 MLB		SYNC DATE=05/26/2010	
PAGE TITLE			
Ethernet Connector		DRAWING NUMBER	SIZE
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Page Notes

Power aliases required by this page:

- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

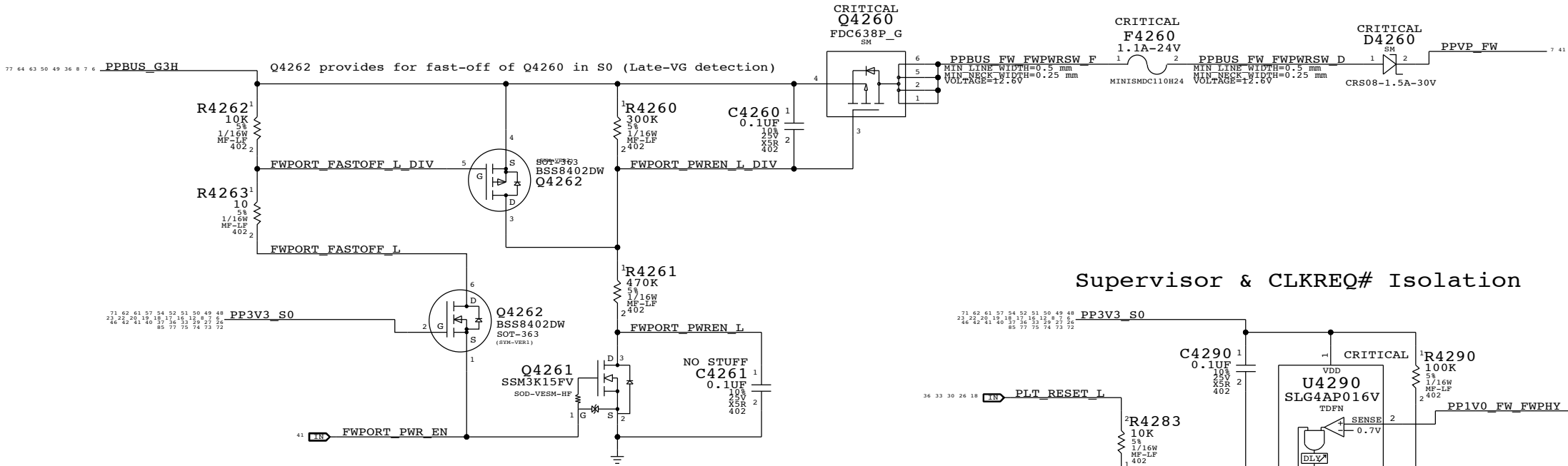
Signal aliases required by this page:

- =FW_CLKREQ_L
- =FW_PME_L

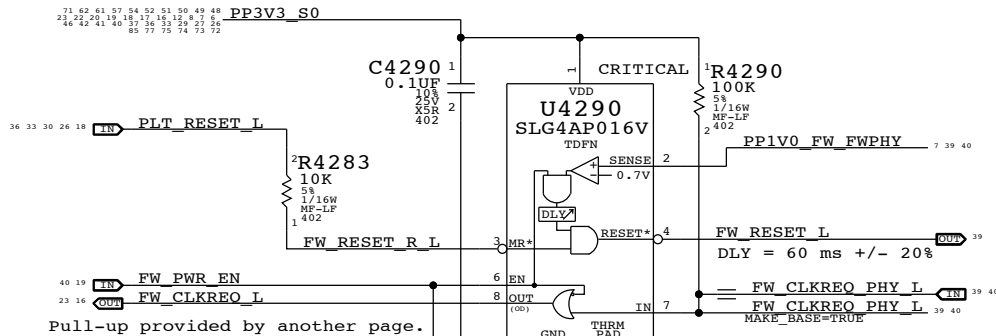
BOM options provided by this page:

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FireWire Port Power Switch

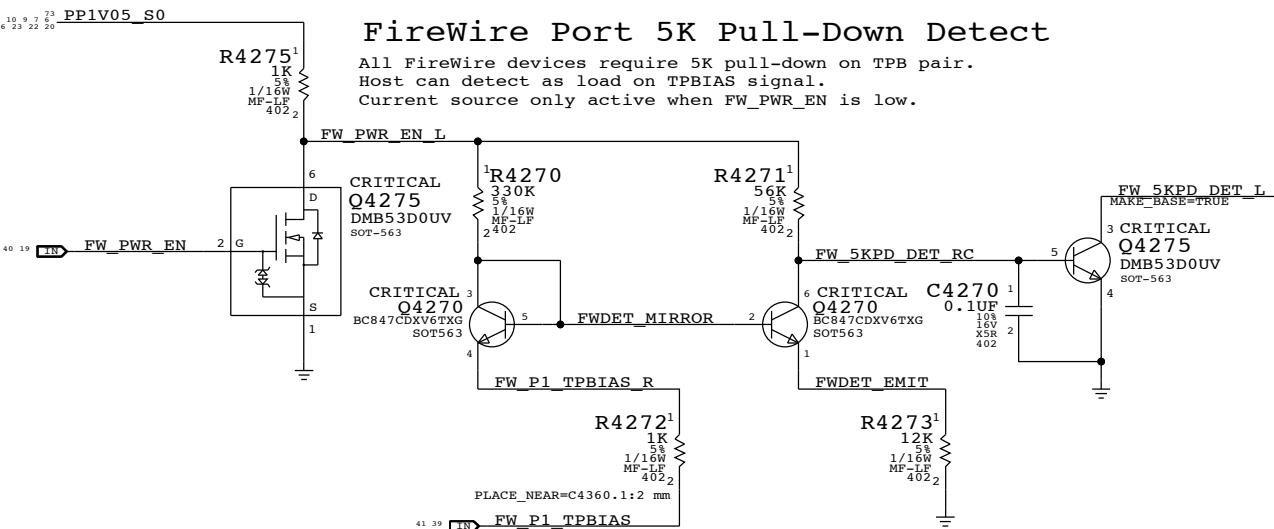


Supervisor & CLKREQ# Isolation



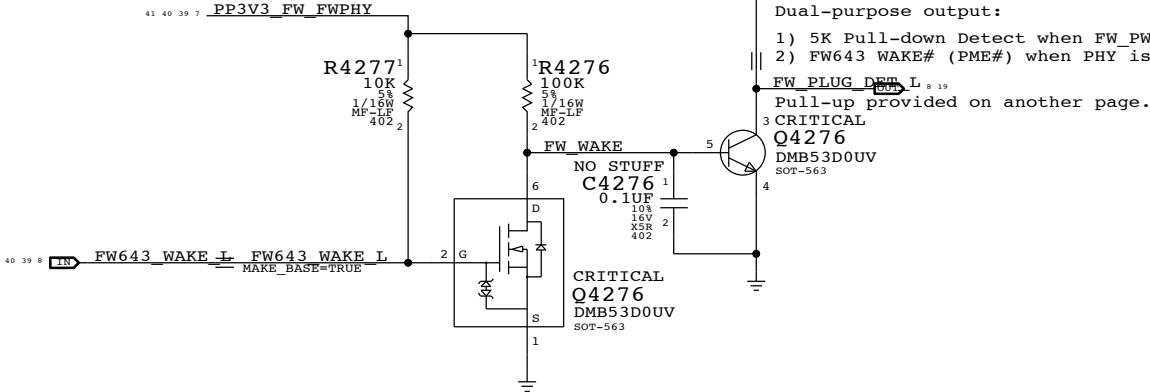
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

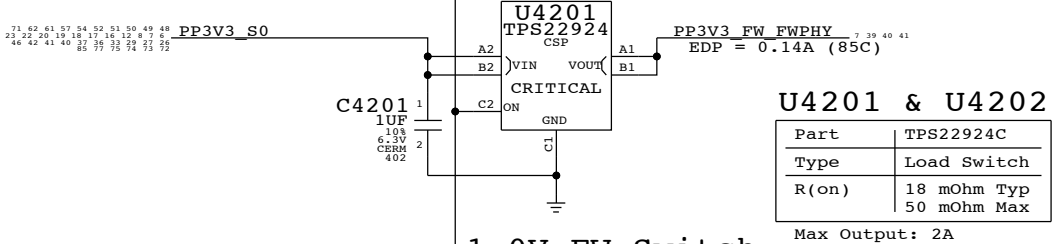


Dual-purpose output:

- 1) 5K Pull-down Detect when FW_PWR_EN is low.
- 2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

3.3V FW Switch

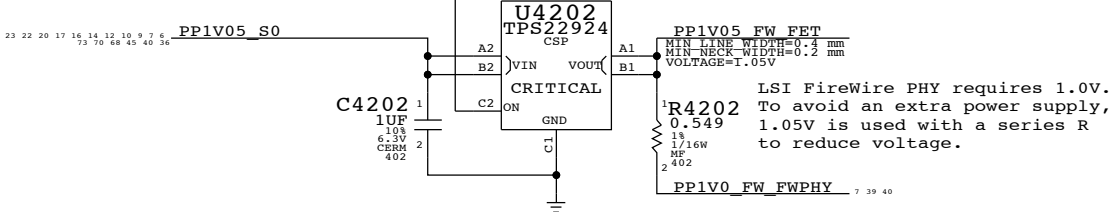


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC MASTER=T27 MLB		SYNC DATE=12/15/2009	
PAGE TITLE		FireWire Port & PHY Power	
		DRAWING NUMBER	SIZE
		REVISION	D
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		42 OF 109	40 OF 86

Page Notes

Power aliases required by this page:

- PPVP_FW_PORT1
- PPVP_FW_PHY_CPS_FET (From Port)
- PPVP_FW_PHY_CPS (To PHY)
- PP3V3_FW_FWPHY
- PP3V3_S0_FWLATEVG

Signal aliases required by this page:

- FW_PHY_DS0
- FW_PHY_DS1
- FW_PHY_DS2

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

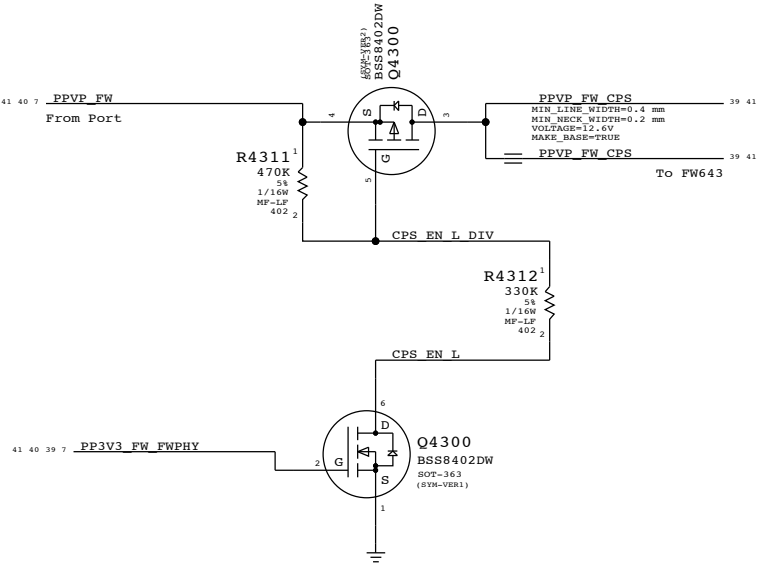
BOM options provided by this page:

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1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

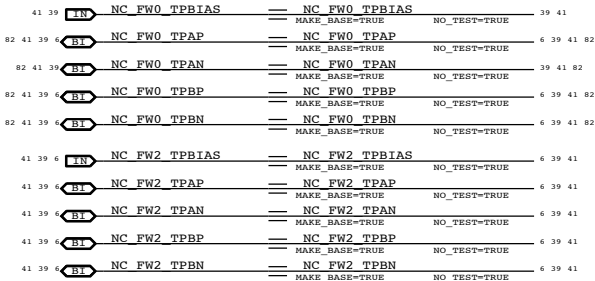
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



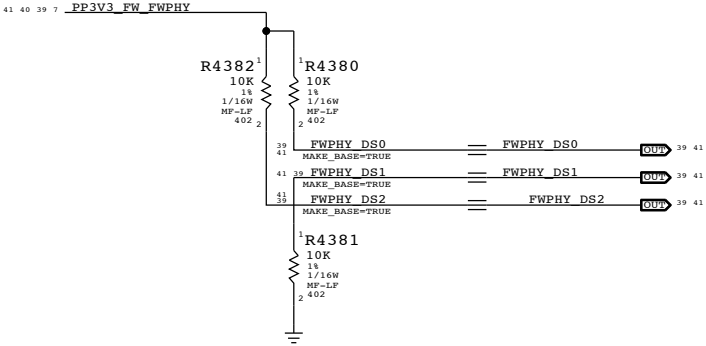
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



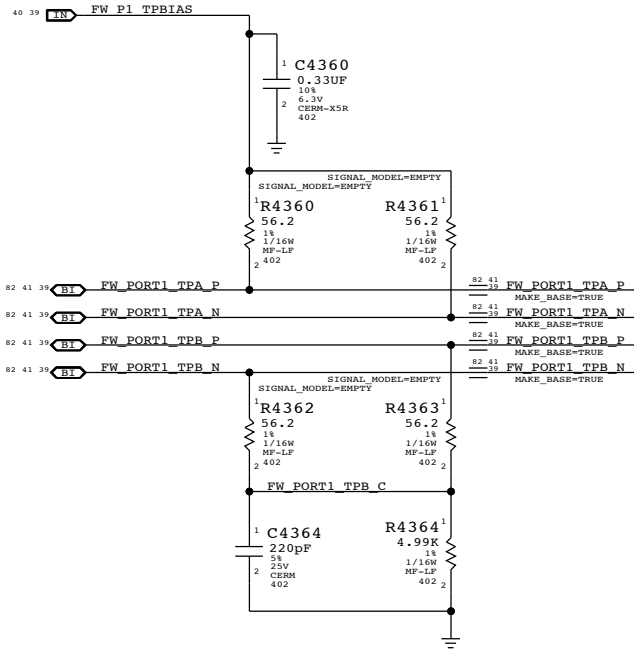
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

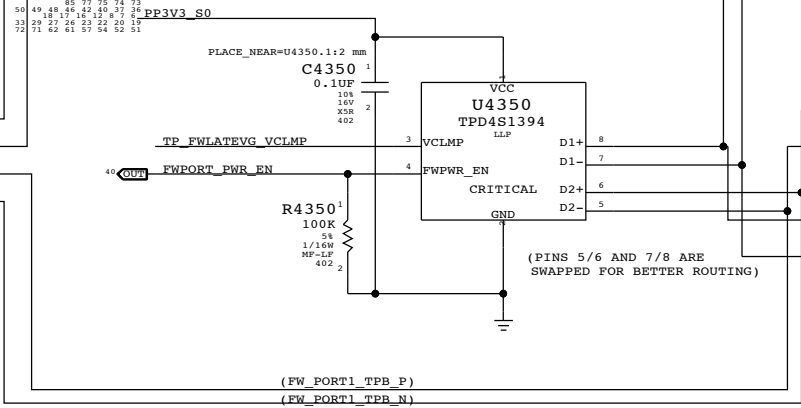


Termination

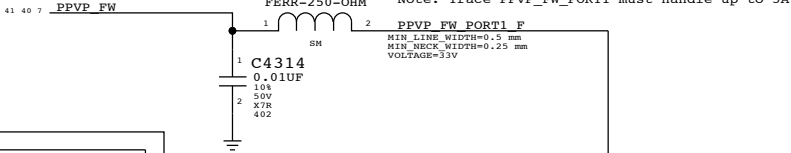
Place close to FireWire PHY



"Snapback" & "Late VG" Protection



Cable Power



PORT 1

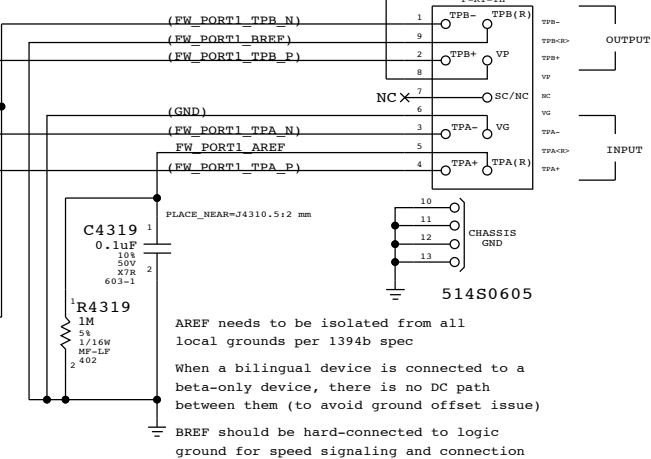
BILINGUAL

CRITICAL

J4310


1394B-M97

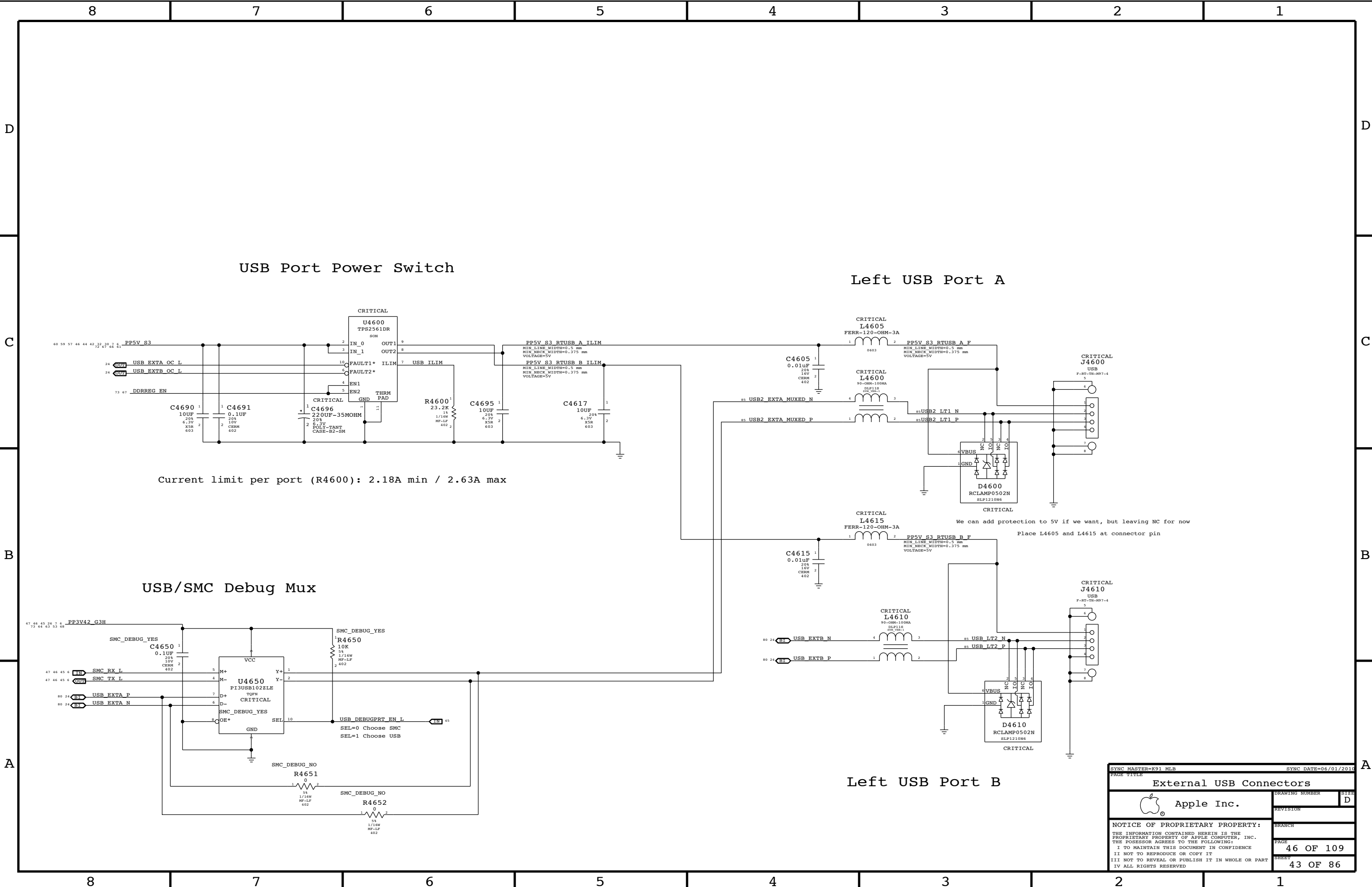
F-RT-TH



AREF needs to be isolated from all local grounds per 1394b spec
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)
BREF should be hard-connected to logic ground for speed signaling and connection


CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

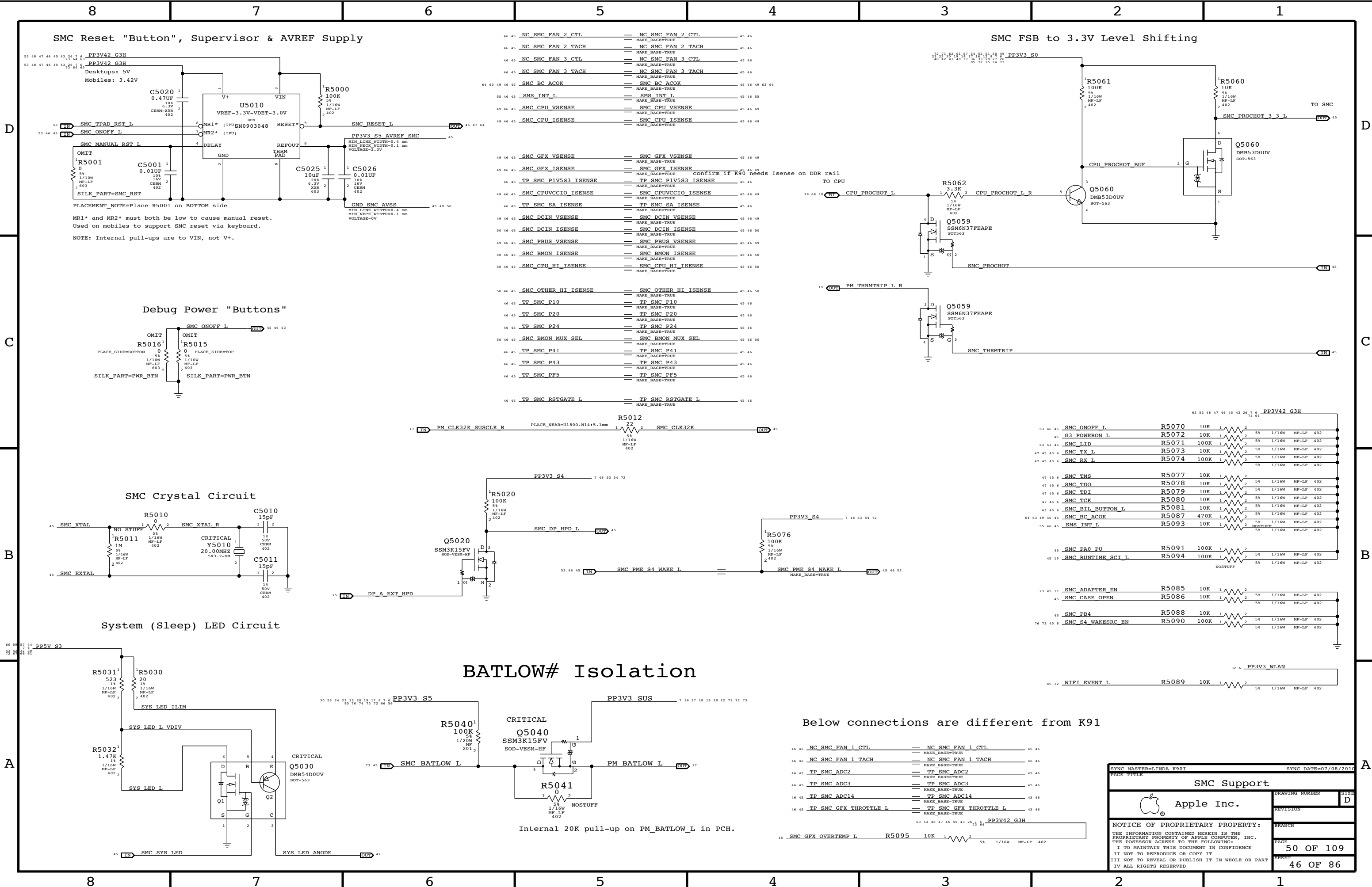
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PAGE TITLE			
FireWire Connector		DRAWING NUMBER	SIZE
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		PAGE	43 OF 109
		SHEET	41 OF 86



Current limit per port (R4600): 2.18A min / 2.63A max

We can add protection to 5V if we want, but leaving NC for now
Place L4605 and L4615 at connector pin

SYNC MASTER=K91 MLB		SYNC DATE=06/01/2010	
PAGE TITLE			
External USB Connectors			
 Apple Inc.		DRAWING NUMBER	SIZE
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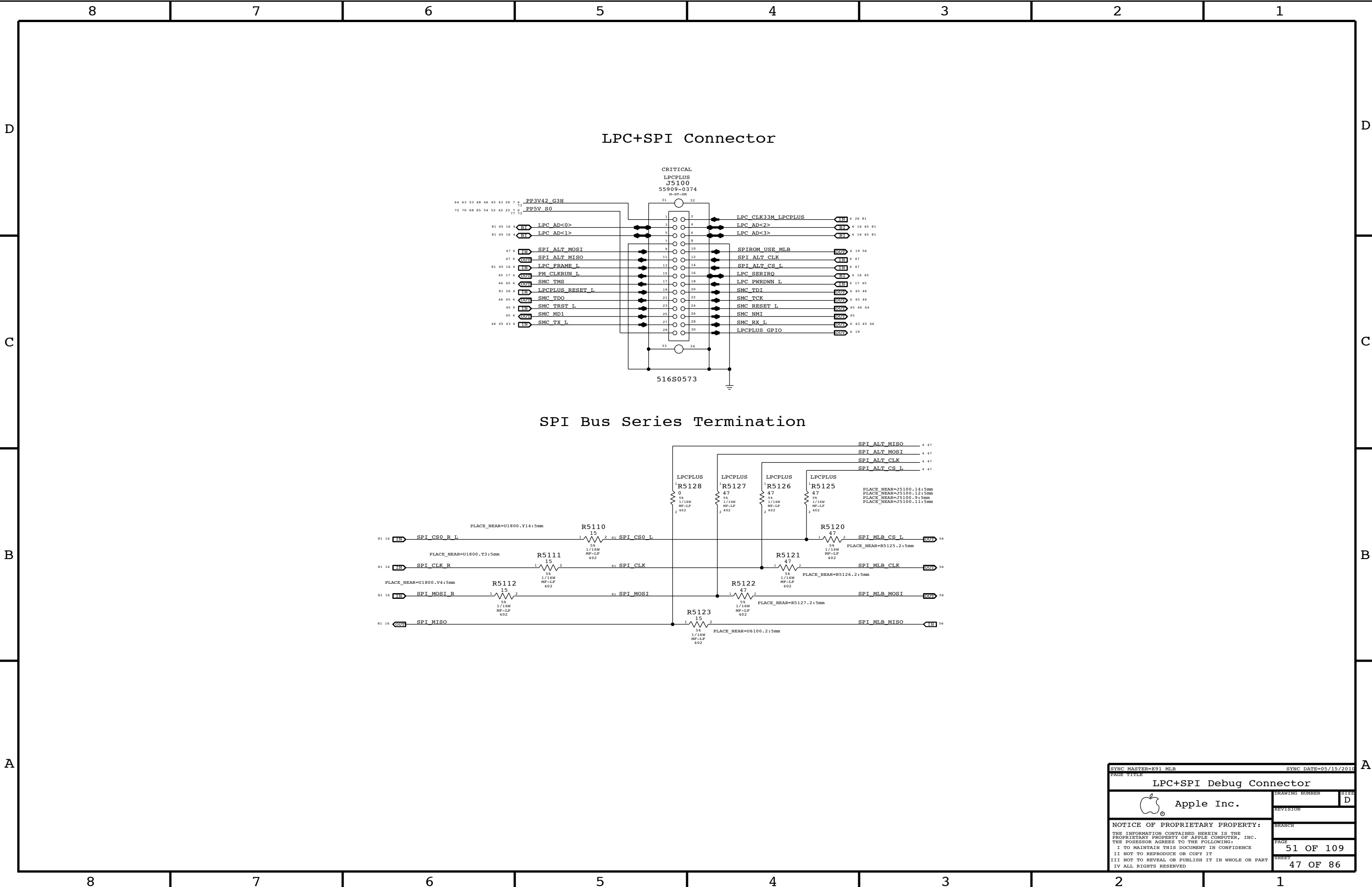
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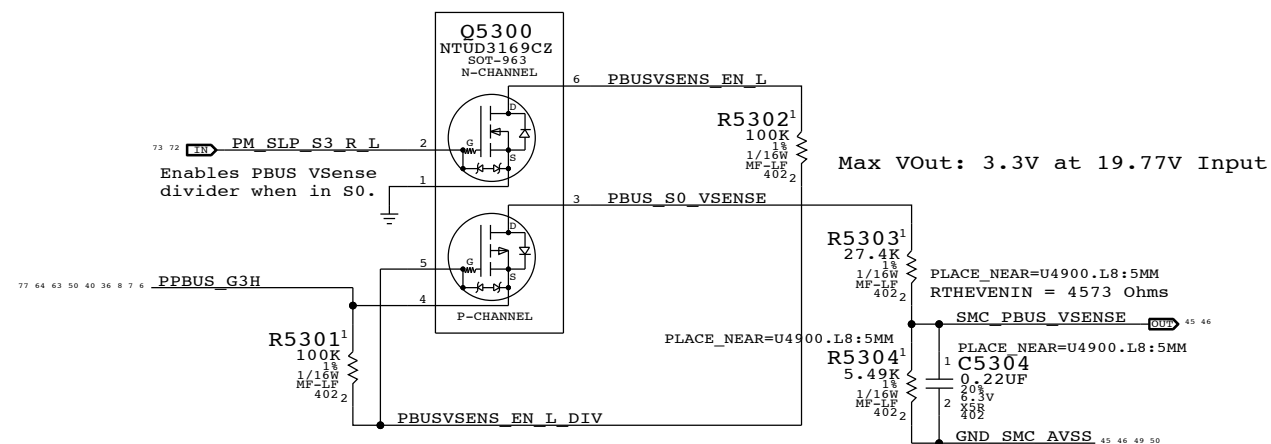
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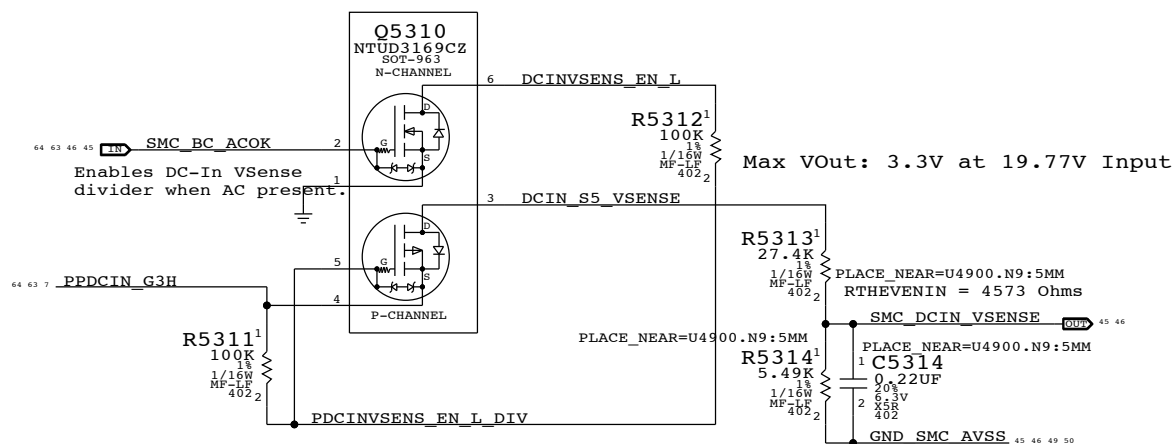
SYNC MASTER=LINDA K901		SYNC DATE=07/08/2010	
PAGE TITLE		PAGE	
SMC Support		DRAWING NUMBER	SIZE D
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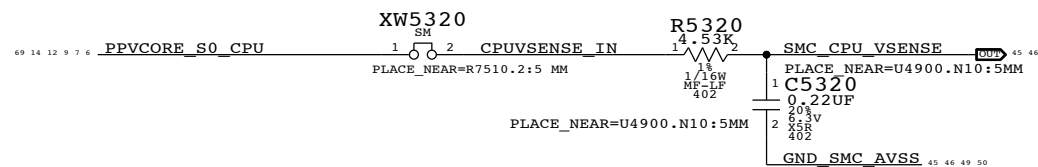
PBUS Voltage Sense Enable & Filter



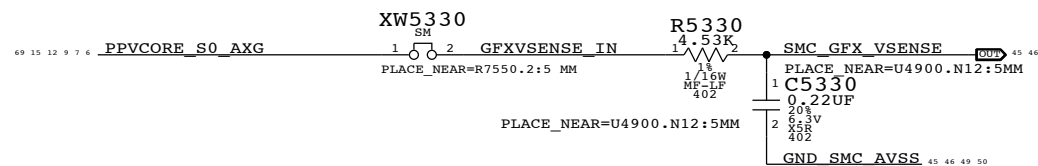
DC-In Voltage Sense Enable & Filter



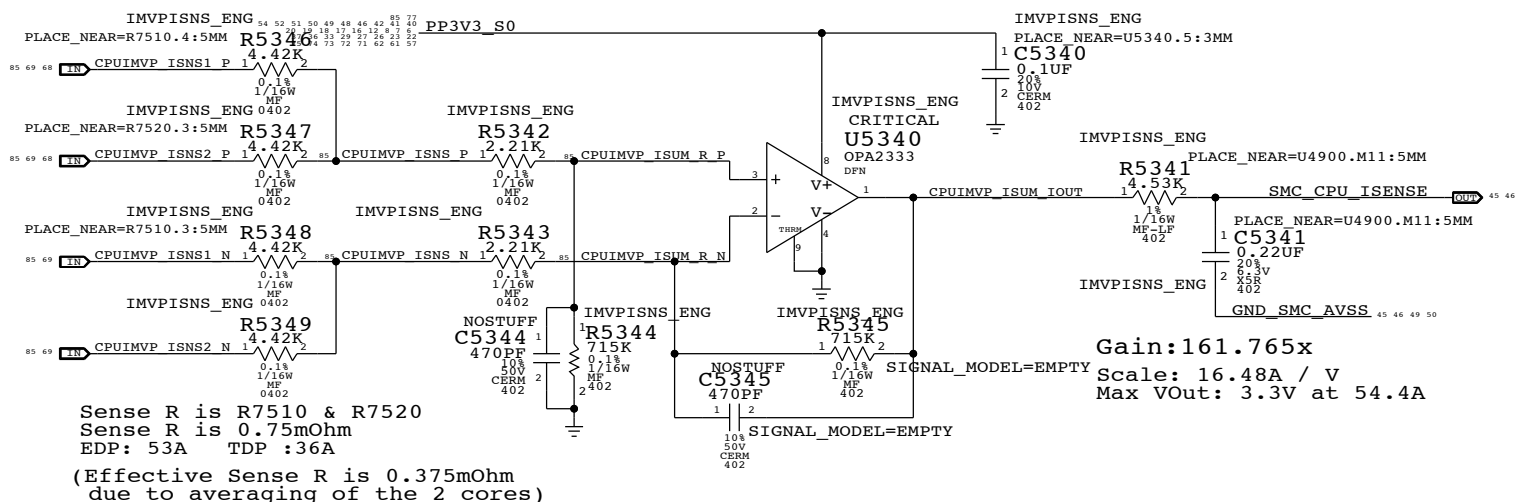
CPU Vcore Voltage Sense / Filter



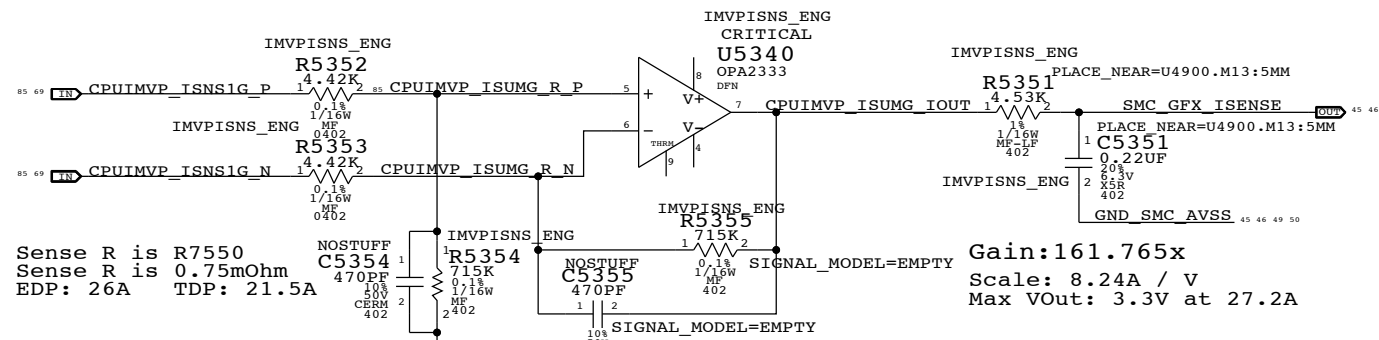
GFX/IG Vcore Voltage Sense / Filter



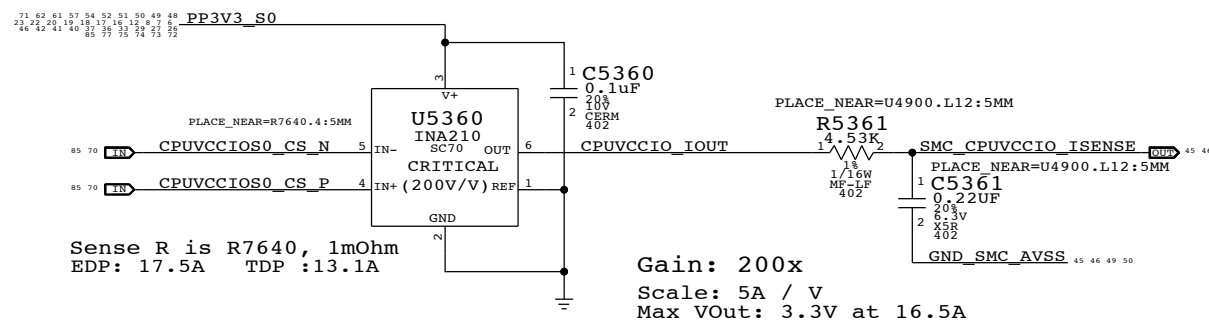
CPU VCore Load Side Current Sense / Filter




GFX/IG VCore Load Side Current Sense / Filter



CPU 1.05V VCCIO Current Sense / Filter



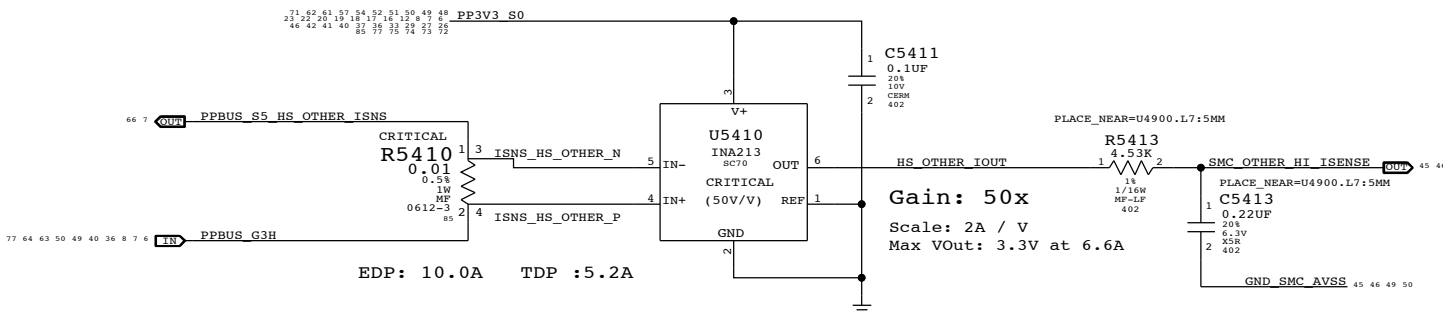
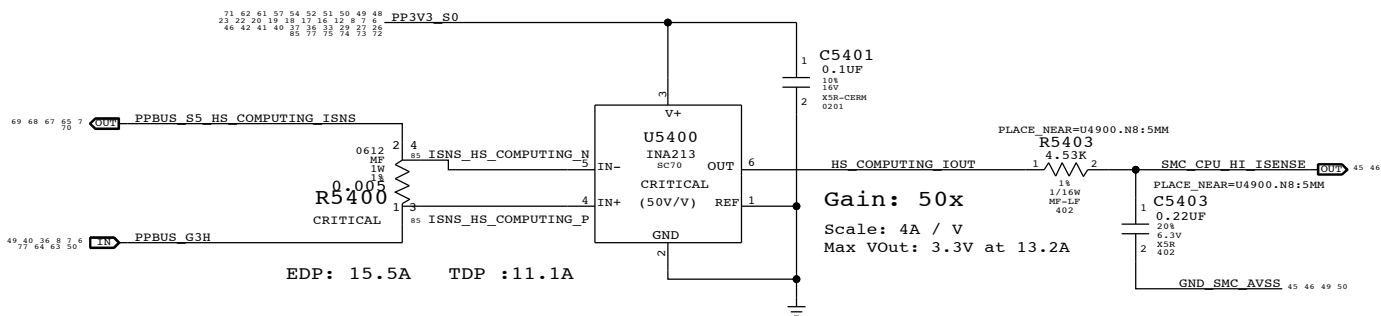
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Voltage & Load Side Current Sensing			
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COMPUTING High Side Current Sense / Filter

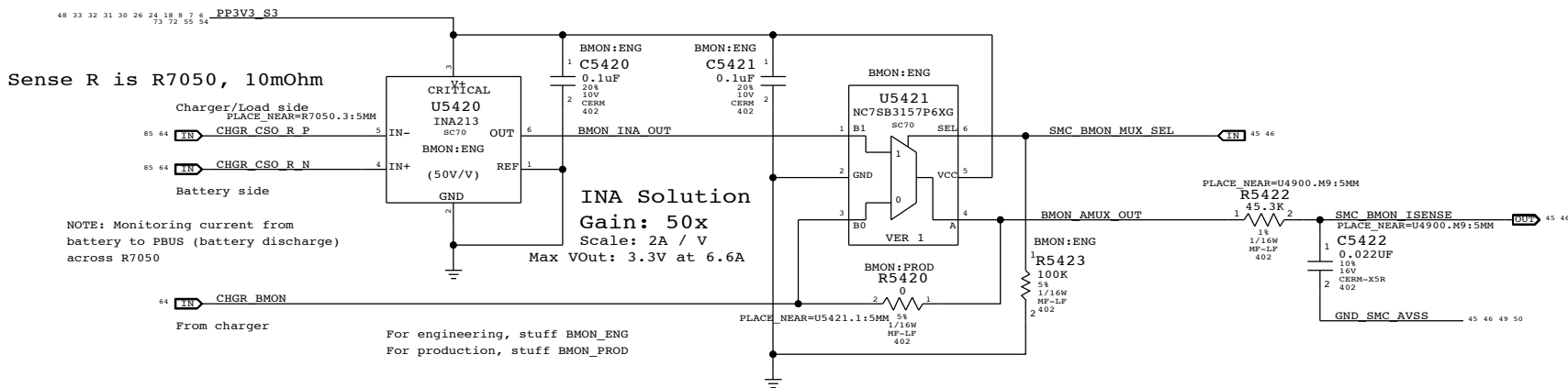
OTHER High Side Current Sense / Filter



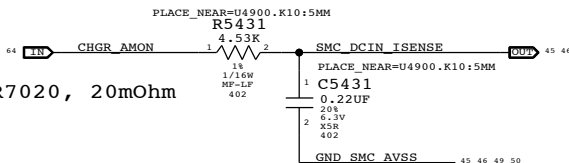
C

C

CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter



DC-IN (AMON) Current Sense Filter



DC-In AMON
ISL6259 Gain: 20x
Scale: 2.5A / V
Max Vout: 3.3V at 8.25A

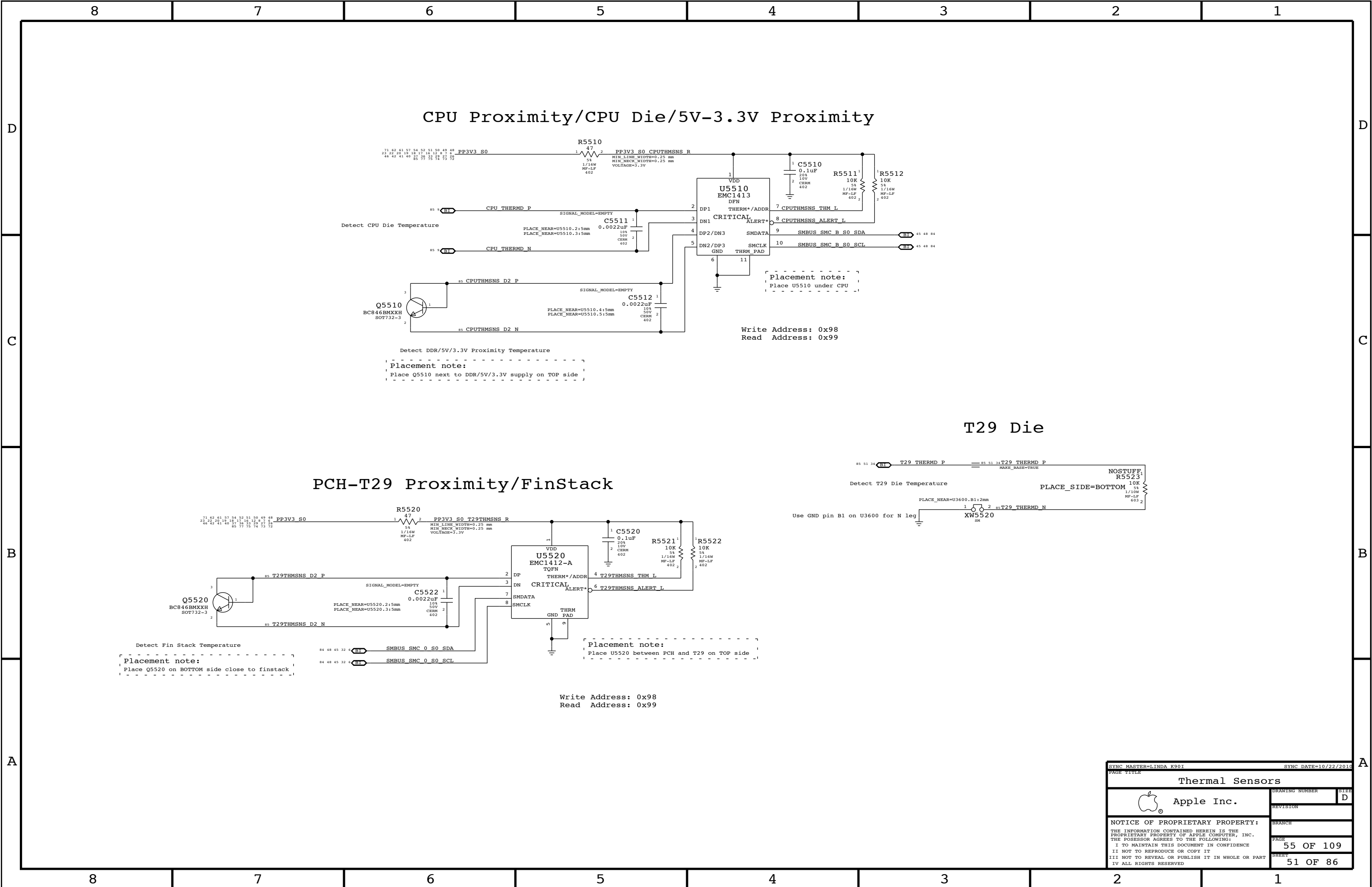
INA (Engineering) Solution
Gain: 50x
Scale: 2A / V
Max Vout: 3.3V at 6.6A

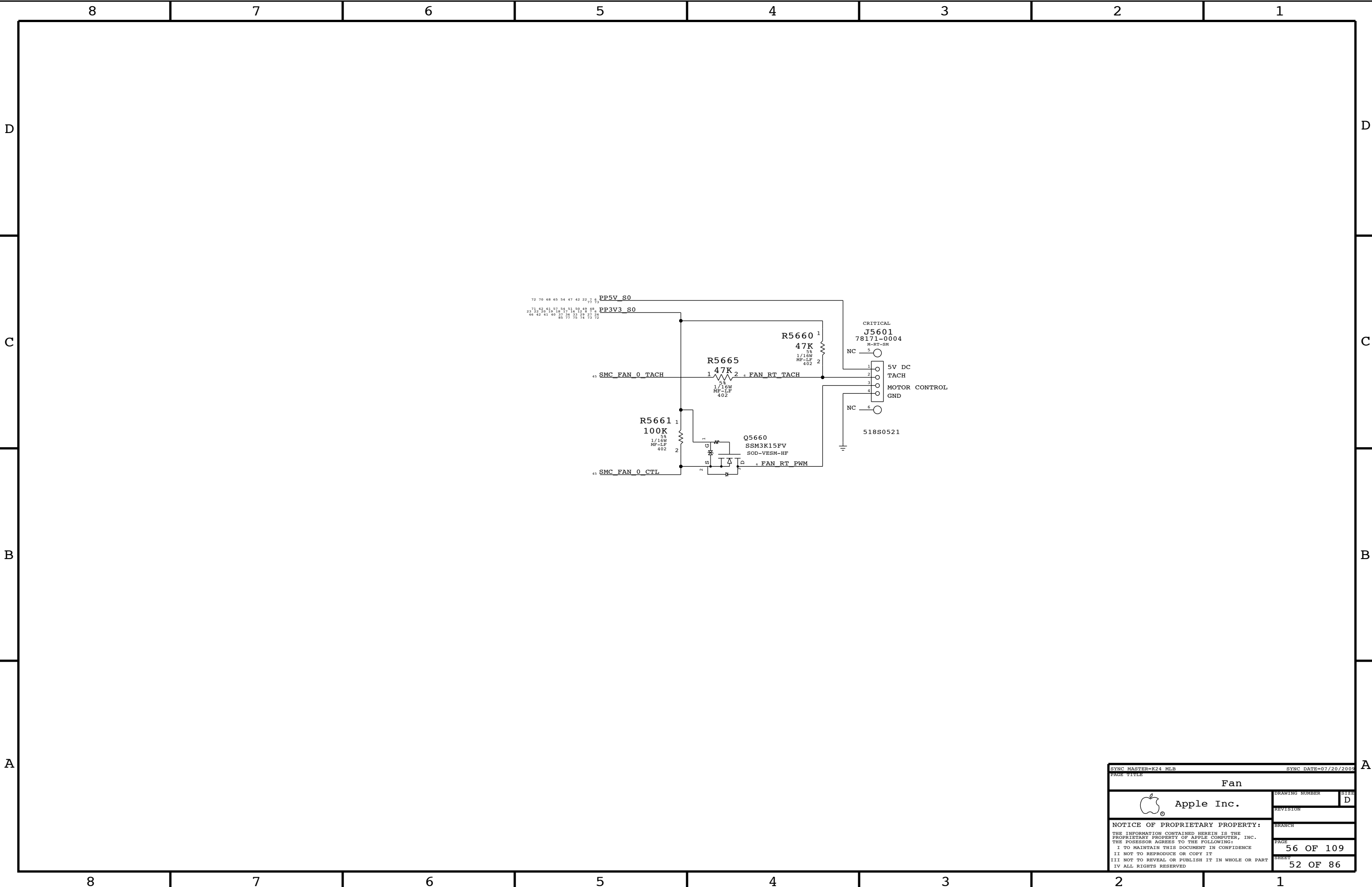
Charger BMON (Production) Solution
ISL6259 Gain: 36x
Scale: 2.78A / V
Max Vout: 3.3V at 9.167A

A

A

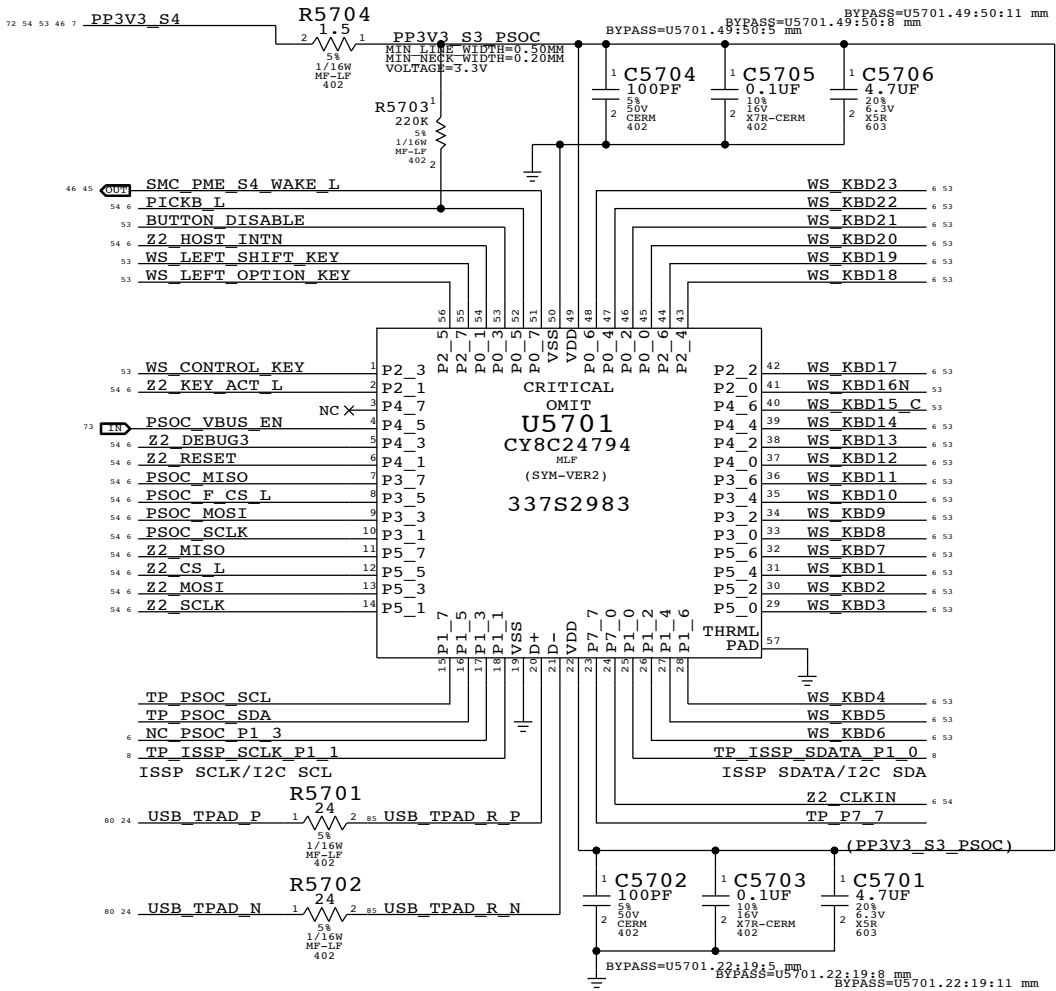
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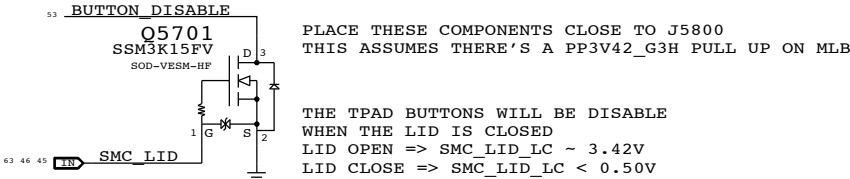


PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

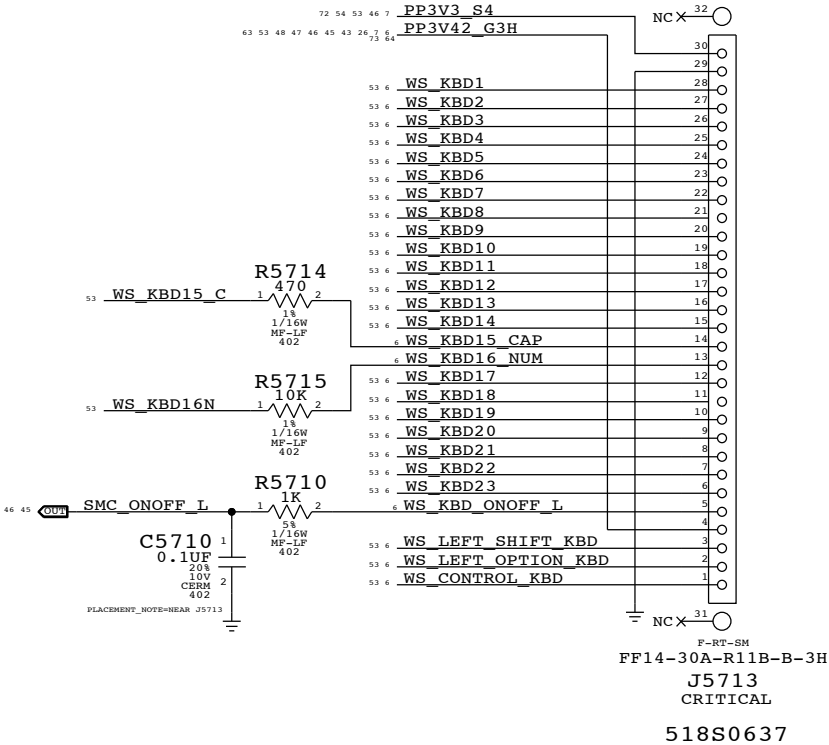


TPAD Buttons Disable



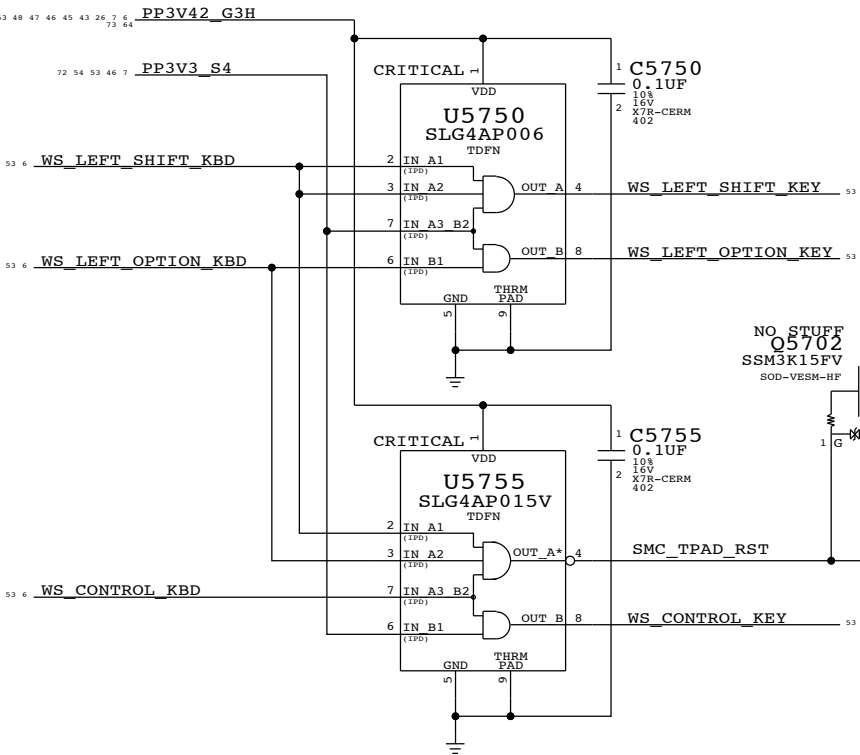
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
	80UA			0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
	14MA (MAX)			0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector



SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.

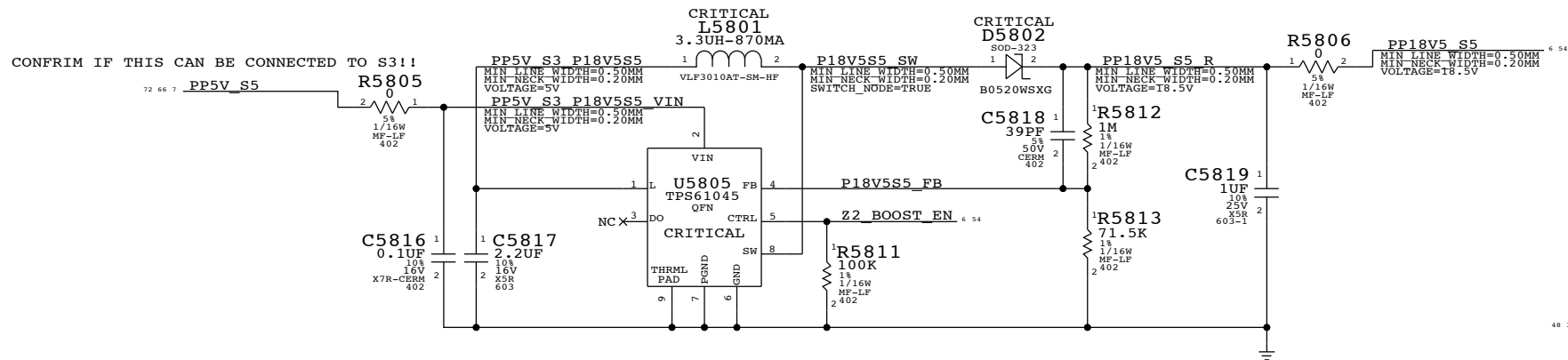


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PAGE TITLE			
WELLSPRING 1		DRAWING NUMBER	SIZE D
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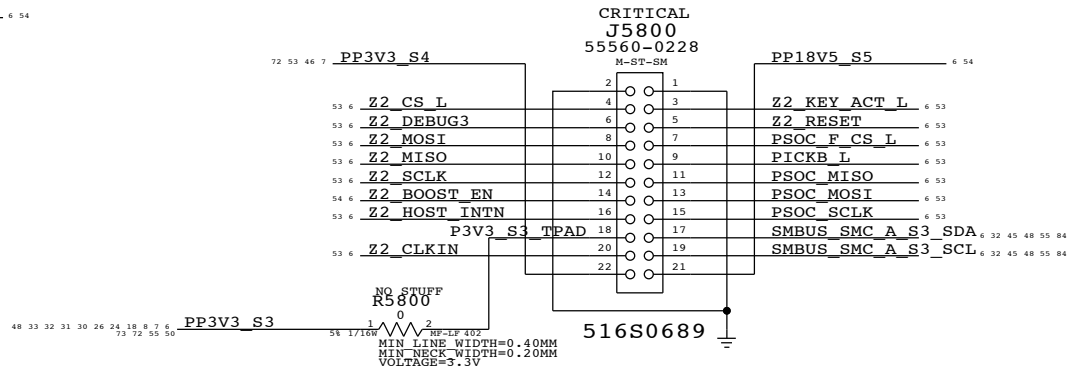
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:

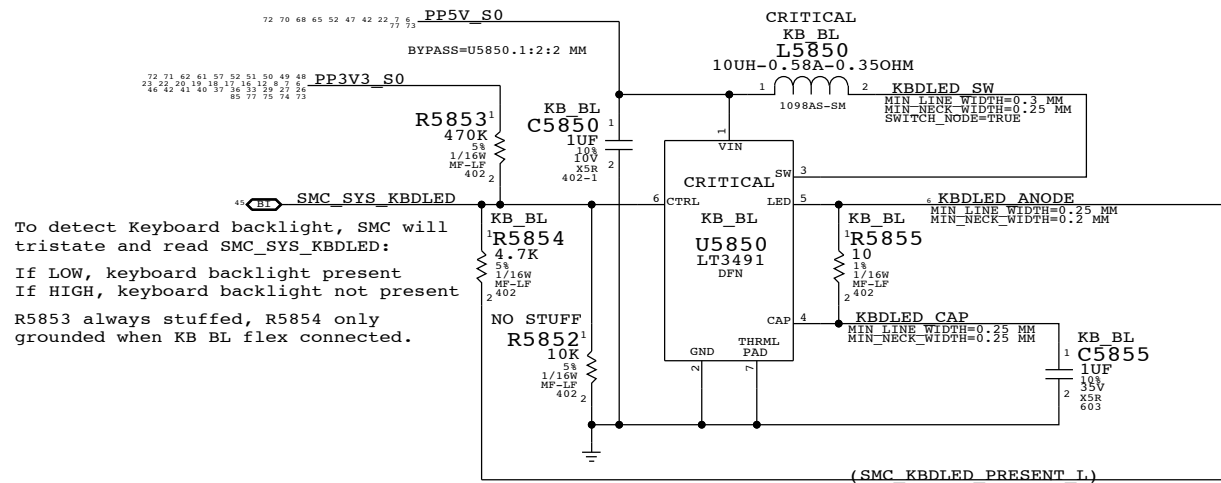
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



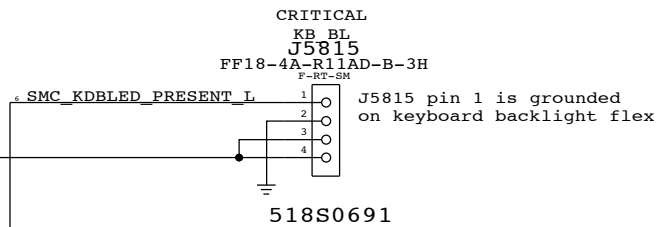
IPD Flex Connector




Keyboard Backlight Driver & Detection

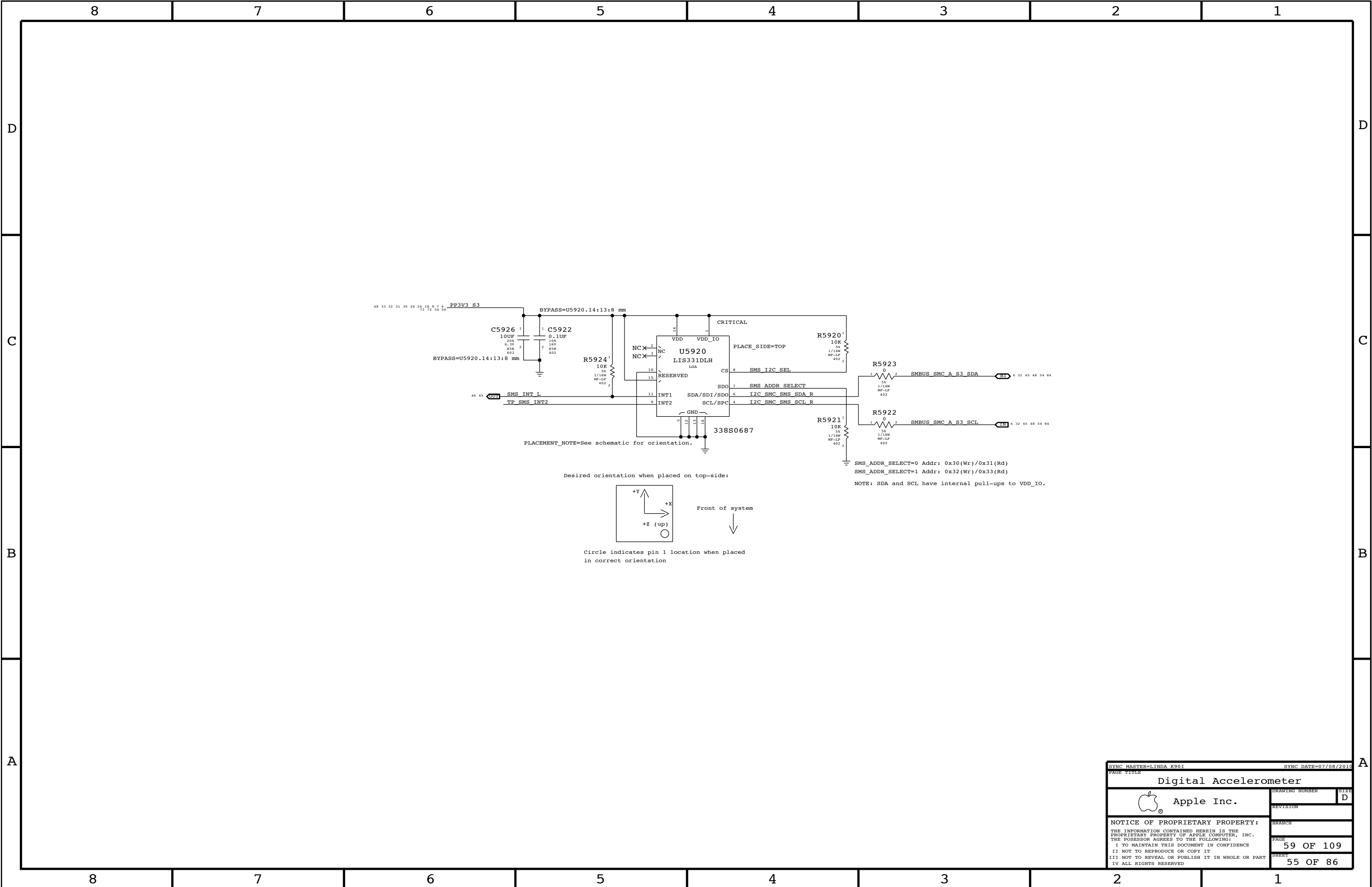


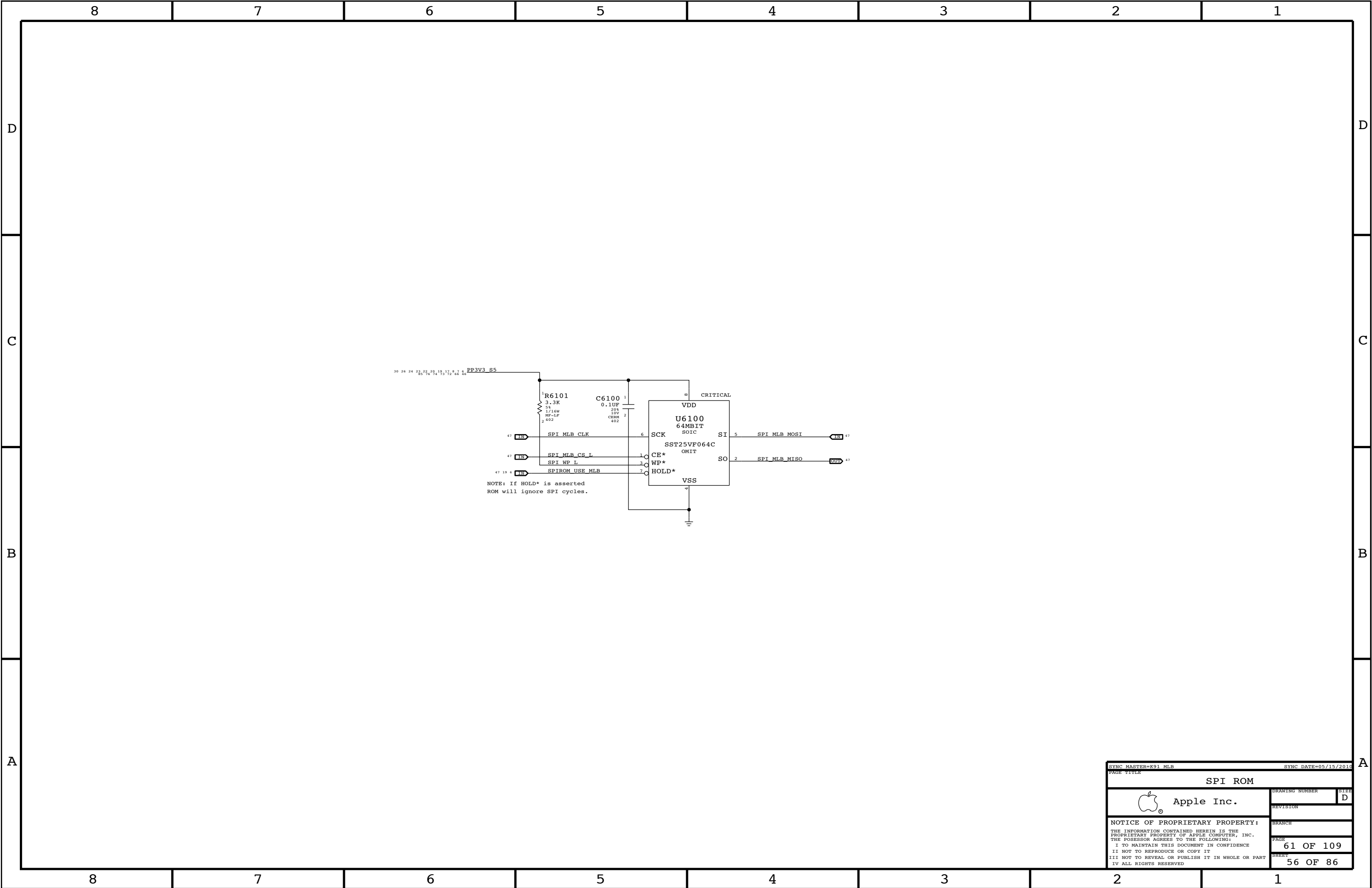
Keyboard Backlight Connector

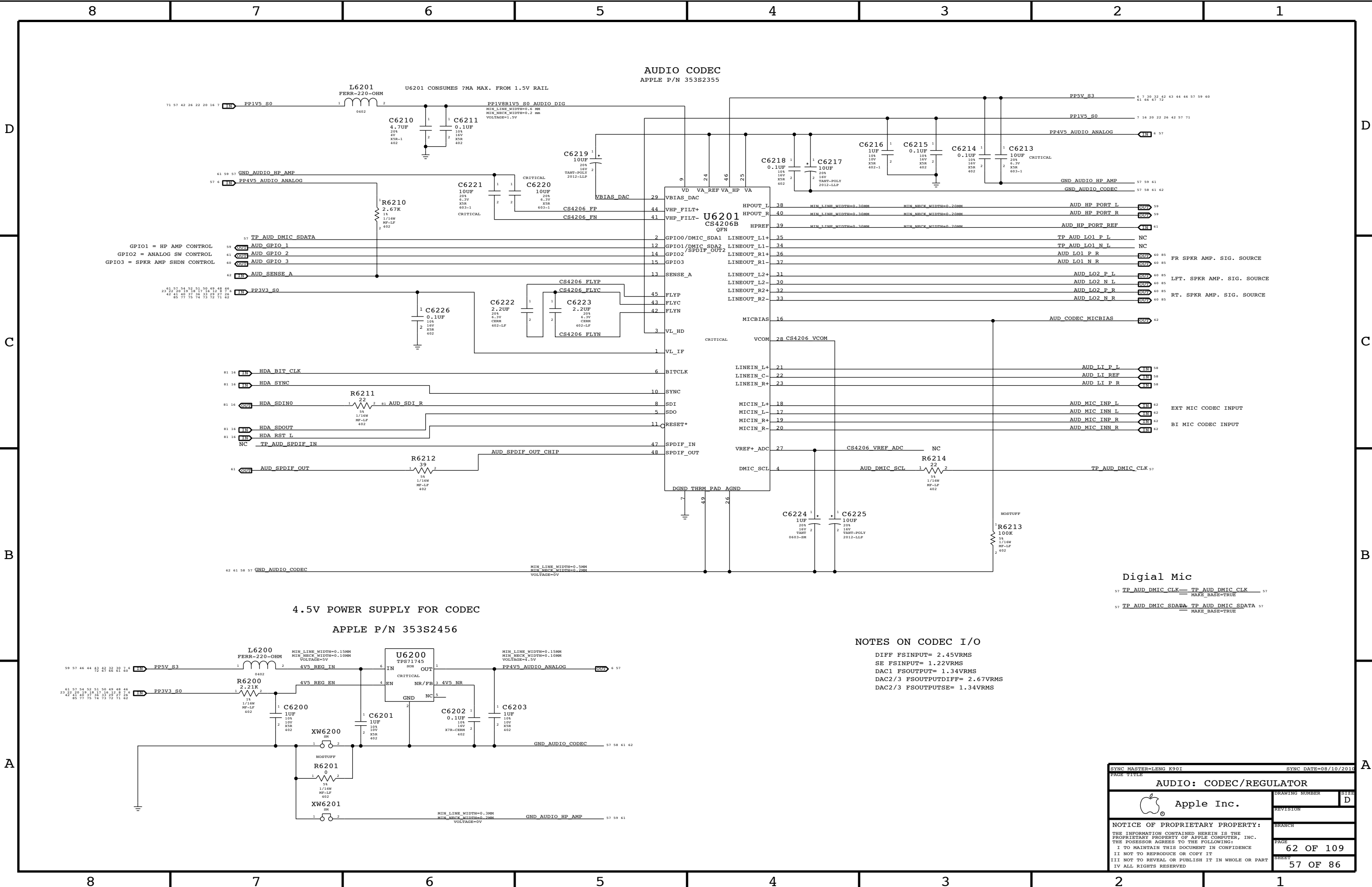


K6 NOTES : C5850 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC MASTER=LINDA K90I		SYNC DATE=07/12/2010	
PAGE TITLE			
WELLSPRING 2			
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Digital Mic

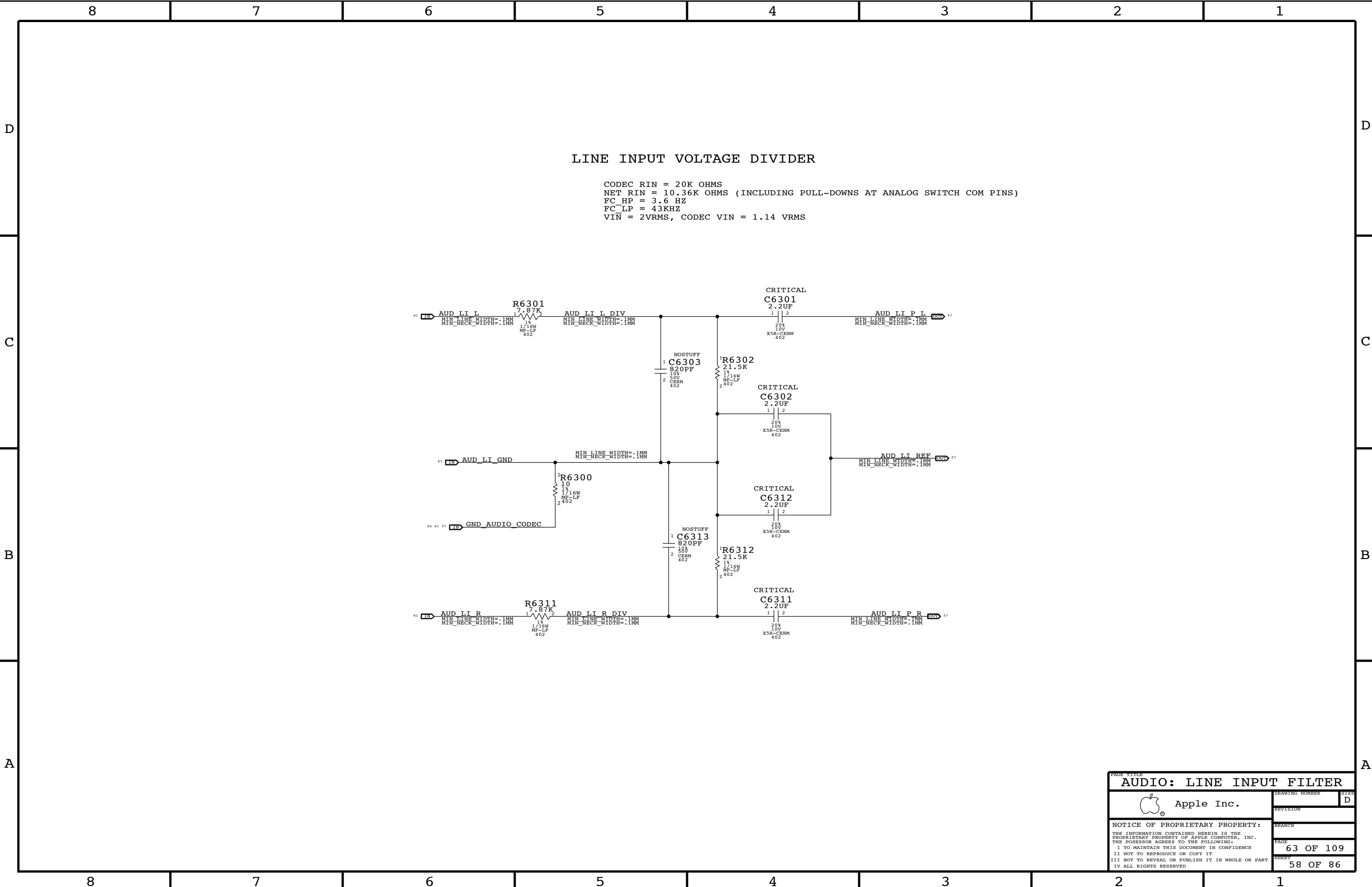
57 TP_AUD_DMIC_CLK TP_AUD_DMIC_CLK 57
MAKE BASE=TRUE

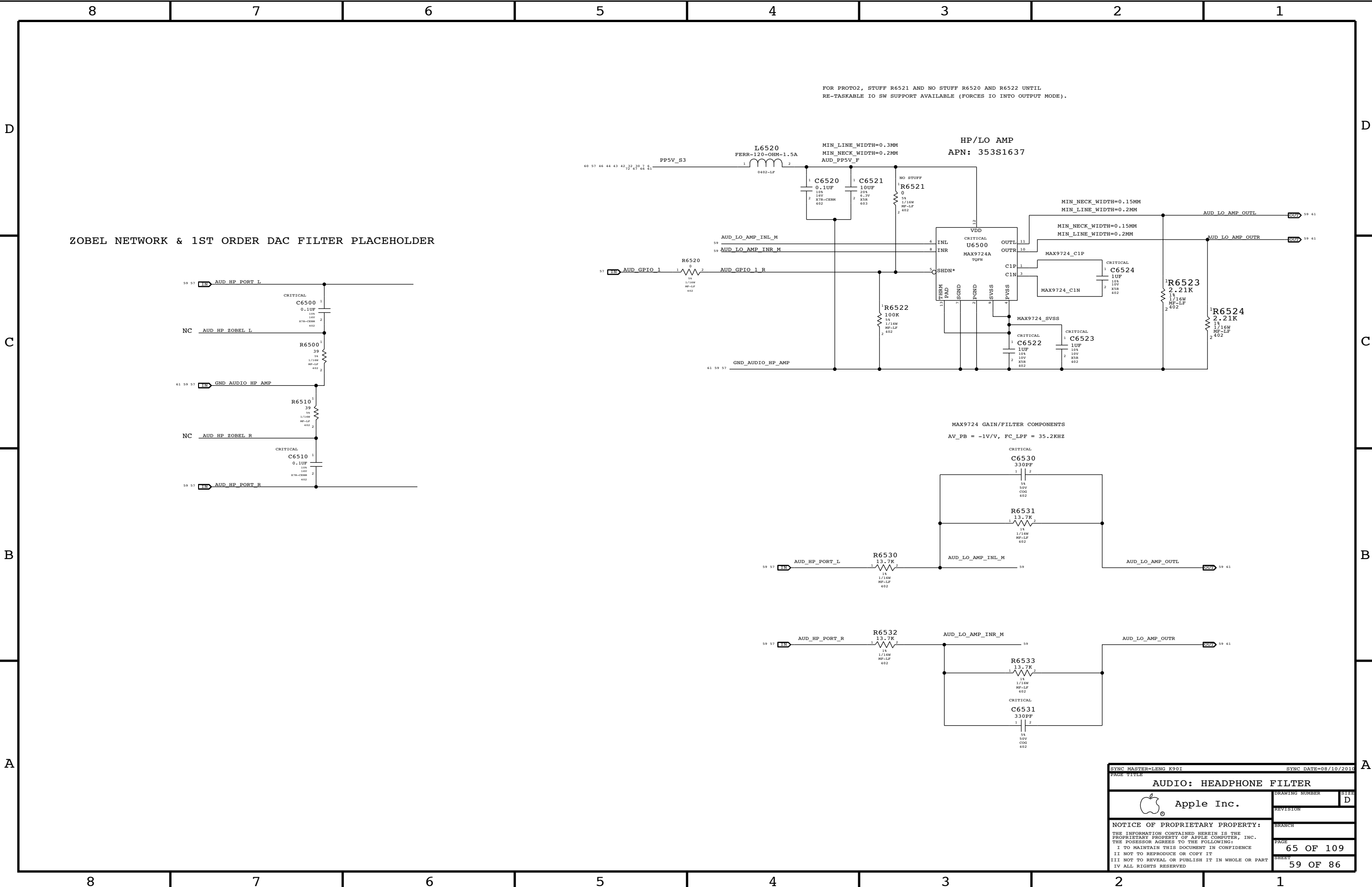
57 TP_AUD_DMIC_SDATA TP_AUD_DMIC_SDATA 57
MAKE BASE=TRUE

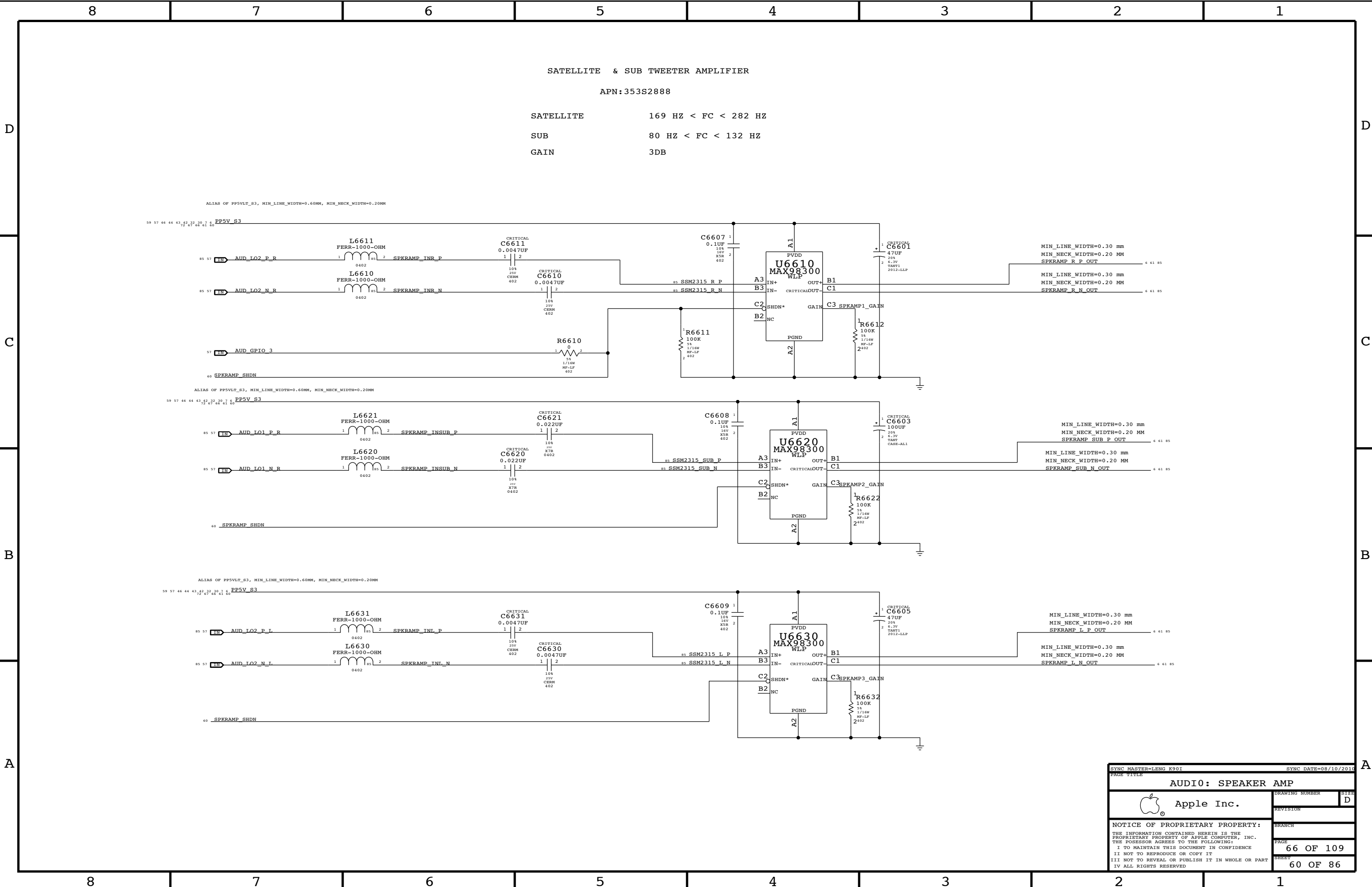
NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

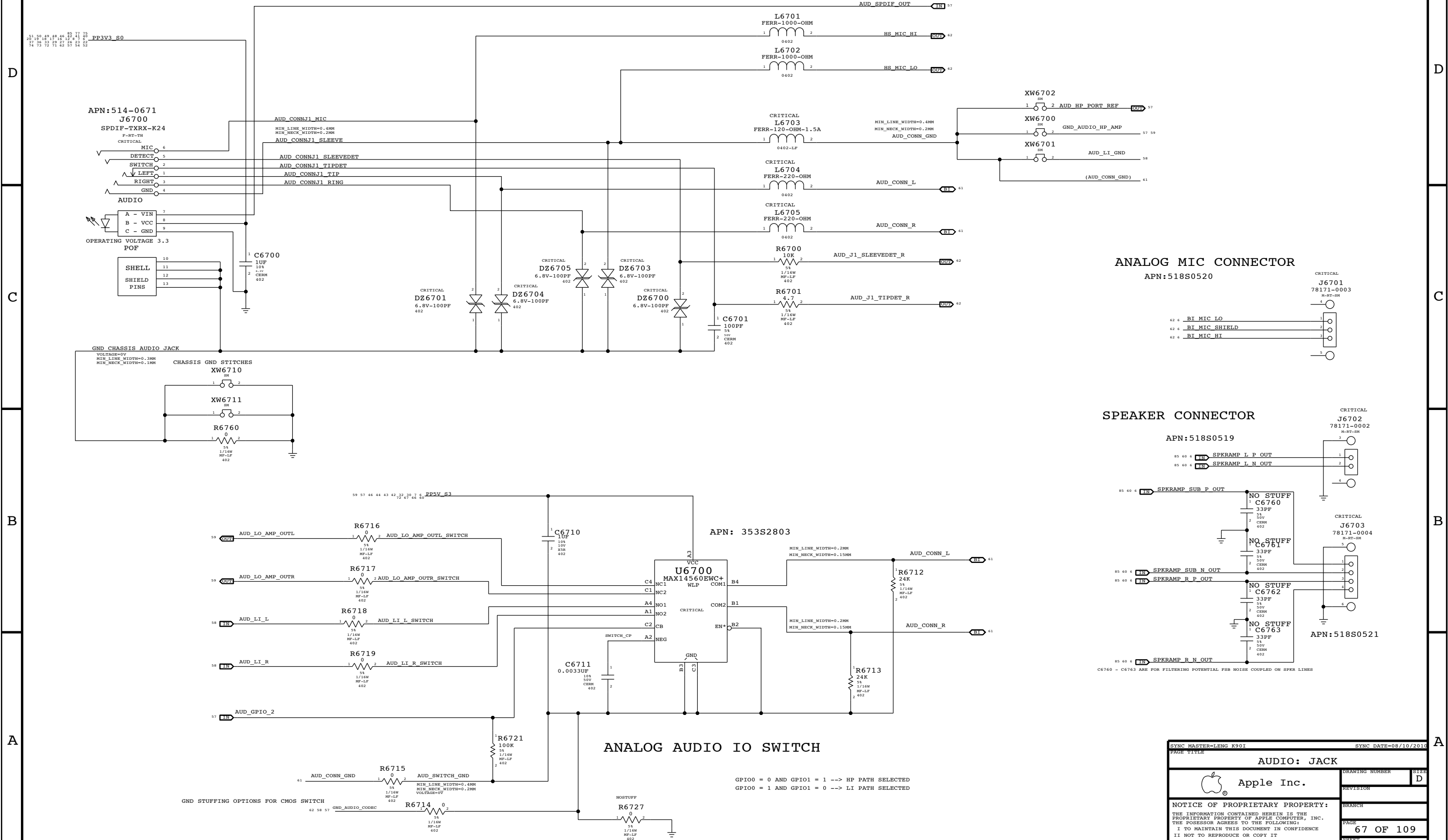
SYNC MASTER=LENG K901		SYNC DATE=08/10/2010	
PAGE TITLE			
AUDIO: CODEC/REGULATOR			
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		REVISION	D
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AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



ANALOG MIC CONNECTOR
APN:518S0520

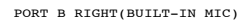
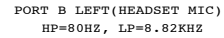
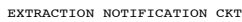
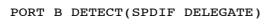
SPEAKER CONNECTOR

SYNC MASTER=LENG K901		SYNC DATE=08/10/2010	
PAGE TITLE		AUDIO: JACK	
Apple Inc.		DRAWING NUMBER	SIZE D
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FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_2 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_2 AND GPIO_1	0X09 (A) AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

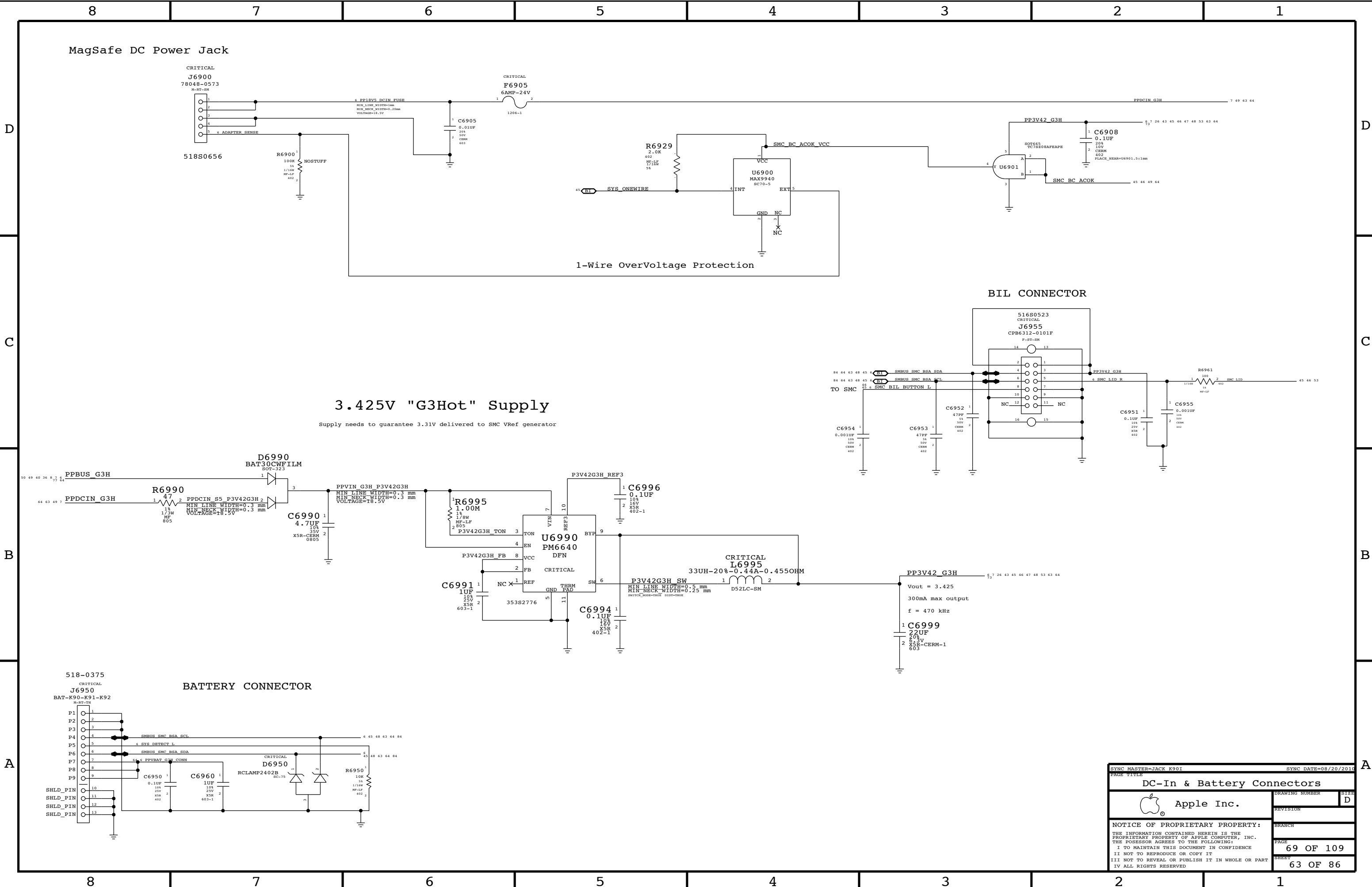
FUNCTION	CONVERTER	PIN	COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)		MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)		MIKEY	MIKEY

FUNCTION	SYSTEM GPIO	SYSTEM INTERRUPT
AUD_IPHS_SWITCH_EN	COUGAR_POINT GPIO16	N/A
AUD_I2C_INT_L	N/A	COUGAR_POINT GPIO5/PIRQH
AUD_IP_PERIPHERAL_DET	N/A	COUGAR_POINT GPIO3/PIRQH

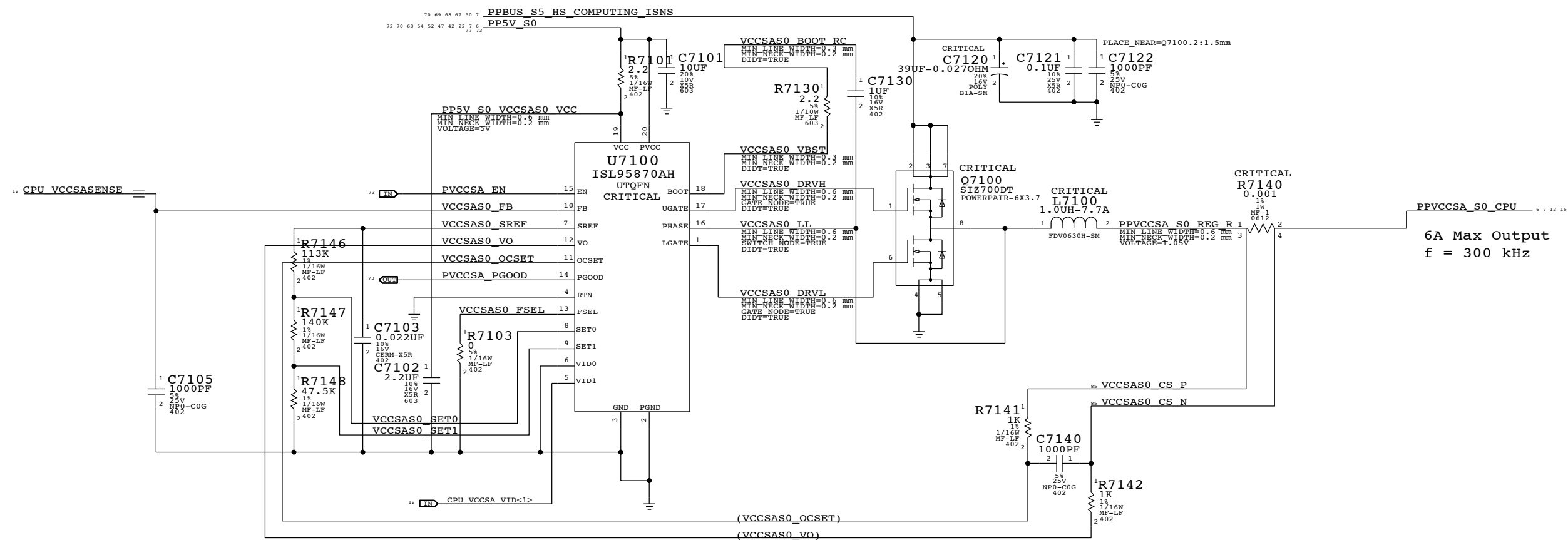



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System Agent Power Supply

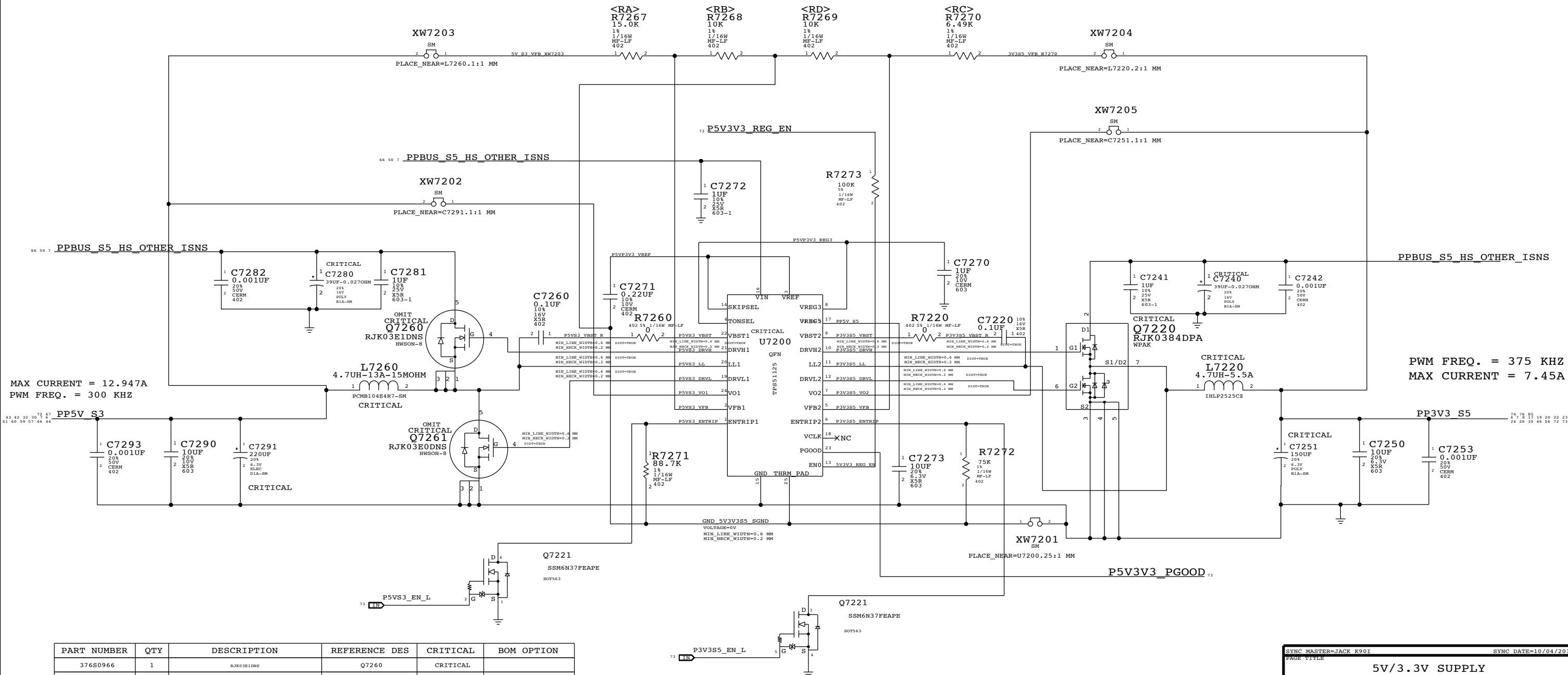


SYNC MASTER=JACK K901		SYNC DATE=08/19/2010	
PAGE TITLE			
System Agent Supply			
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5V_S3/3.3V_S5 POWER SUPPLY

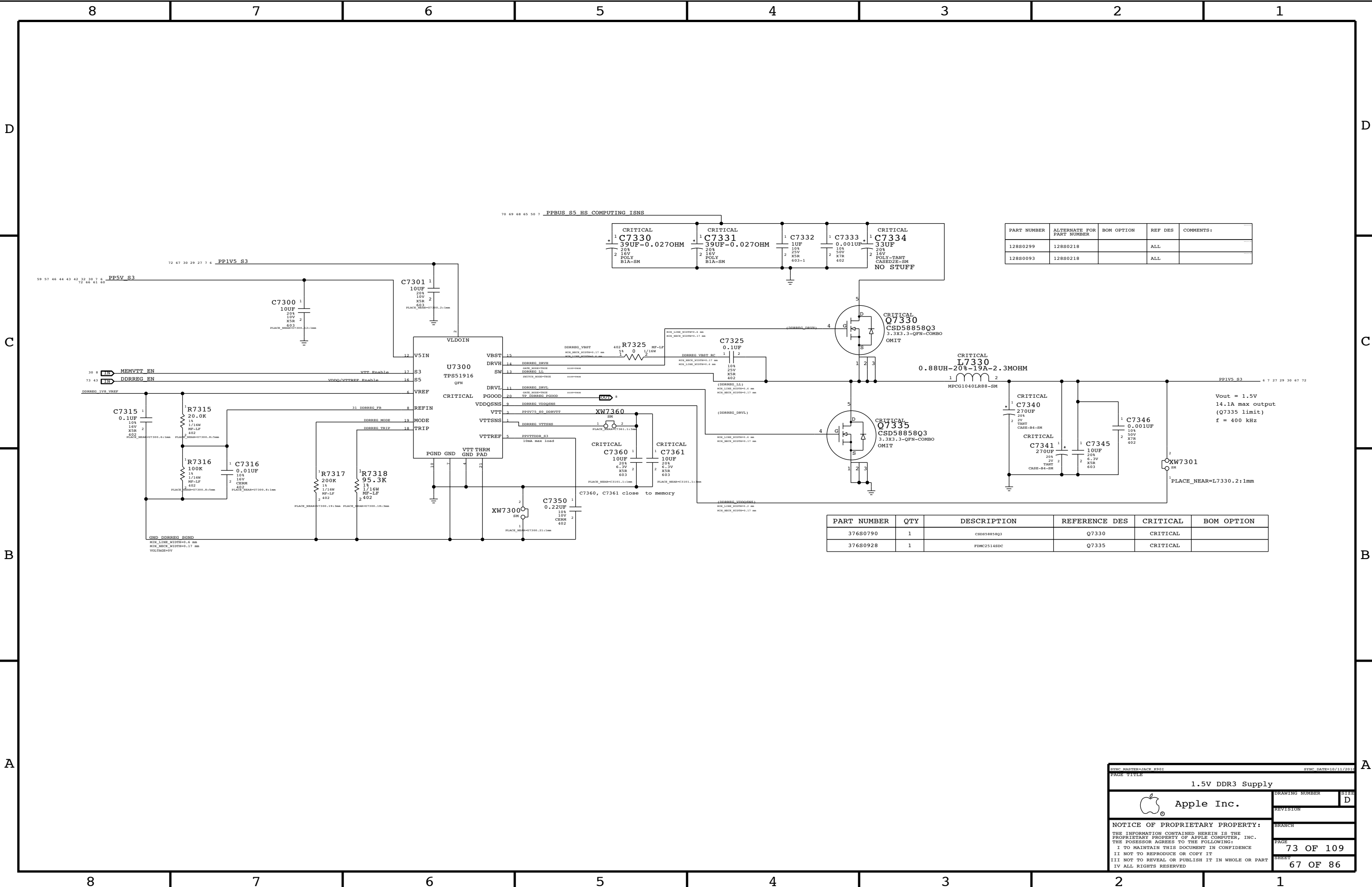
$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$



SEPARATED MASTER PGOOD FOR BOTH 5V AND 3V3.

SYNC MASTER=JACK K901		SYNC DATE=10/04/2010	
PAGE TITLE			
5V/3.3V SUPPLY			
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0790	1	CSD58858Q3	Q7330	CRITICAL	
376S0928	1	FDMC25148DC	Q7335	CRITICAL	

SYNC PARTS=JACK K902

SYNC DATE=10/11/2016

1.5V DDR3 Supply

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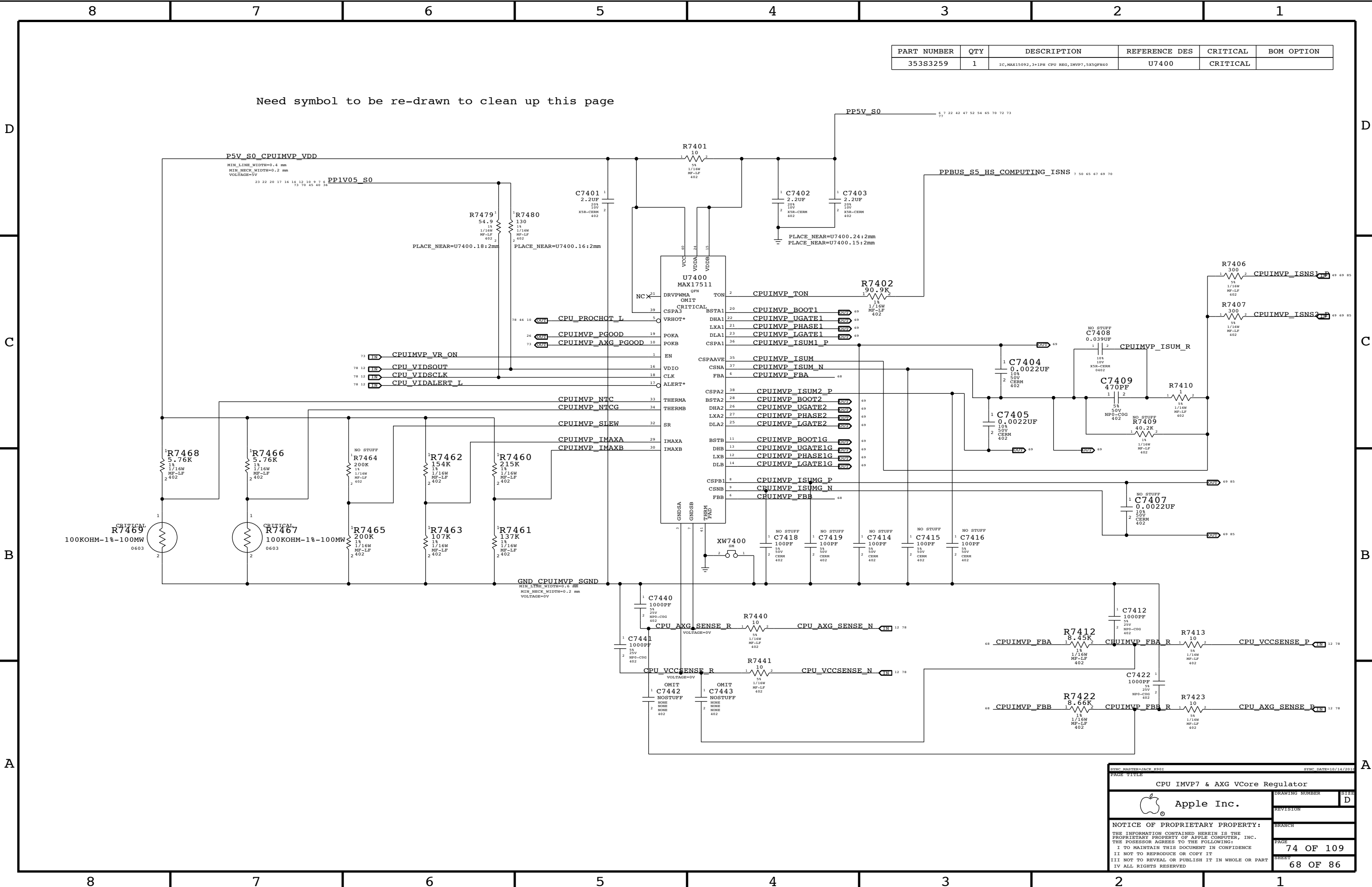
SHEET

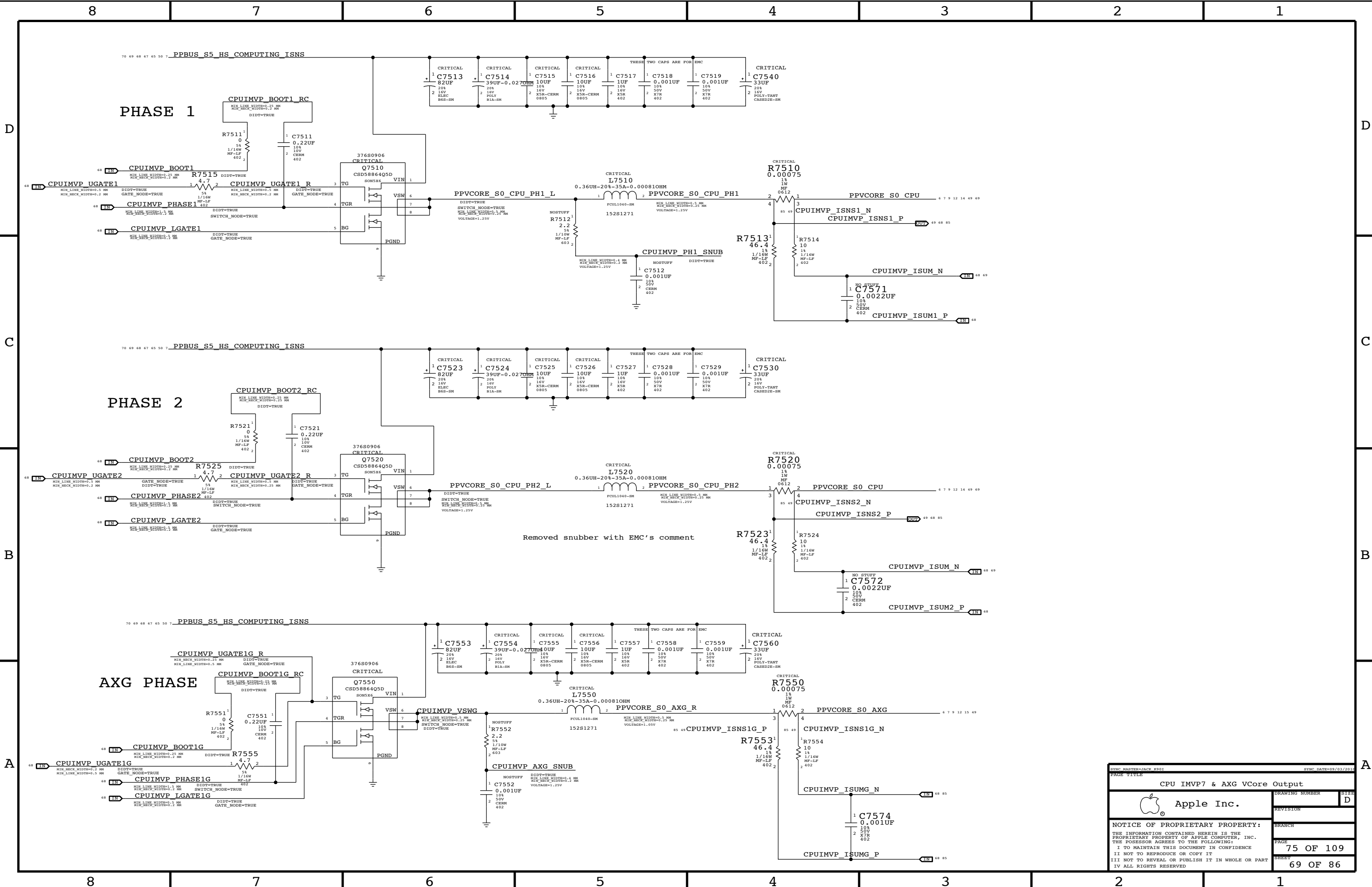
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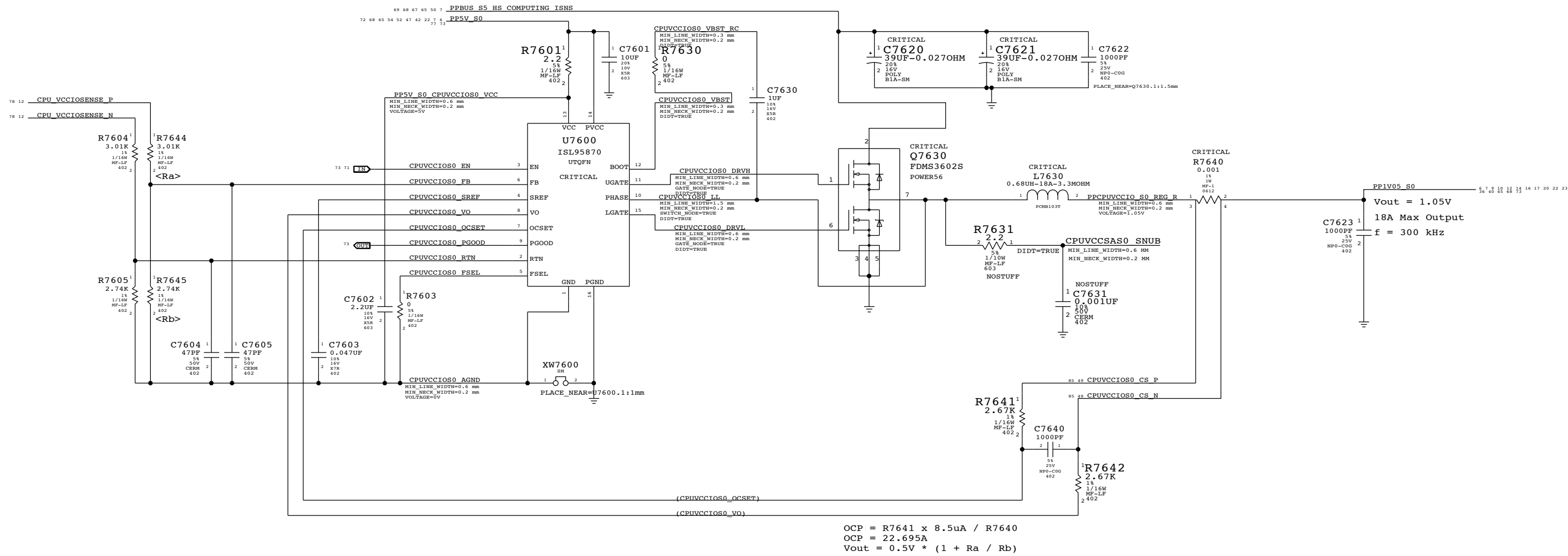
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
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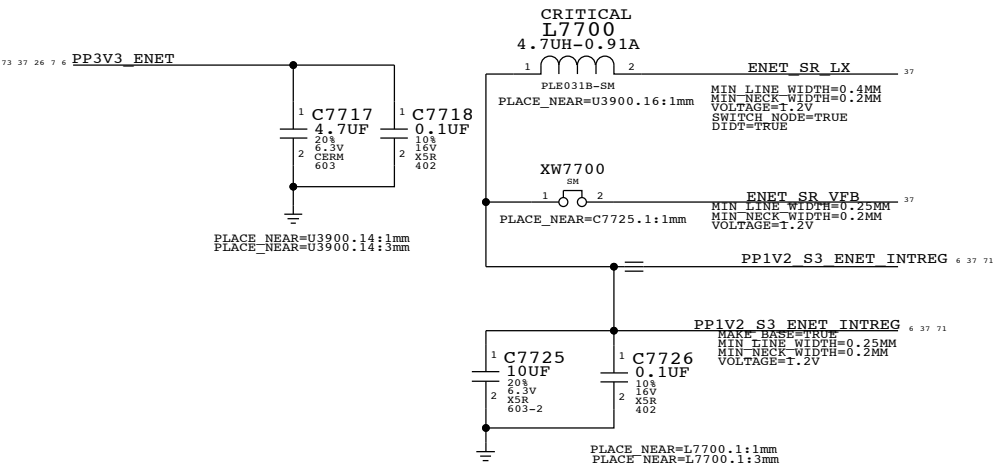


CPU VCCIO (1.05V S0) Regulator



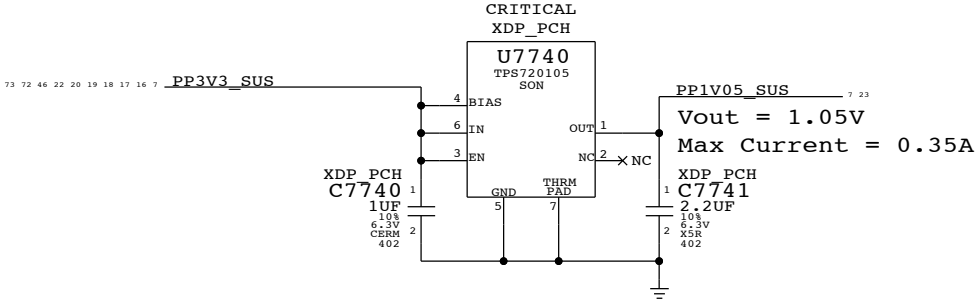
SYNC MASTER=JACK K901		SYNC DATE=08/19/2010	
PAGE TITLE			
CPUVCCIO (1.05V) Power Supply			
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CAESAR IV 1.2V INT.VR CMPTS



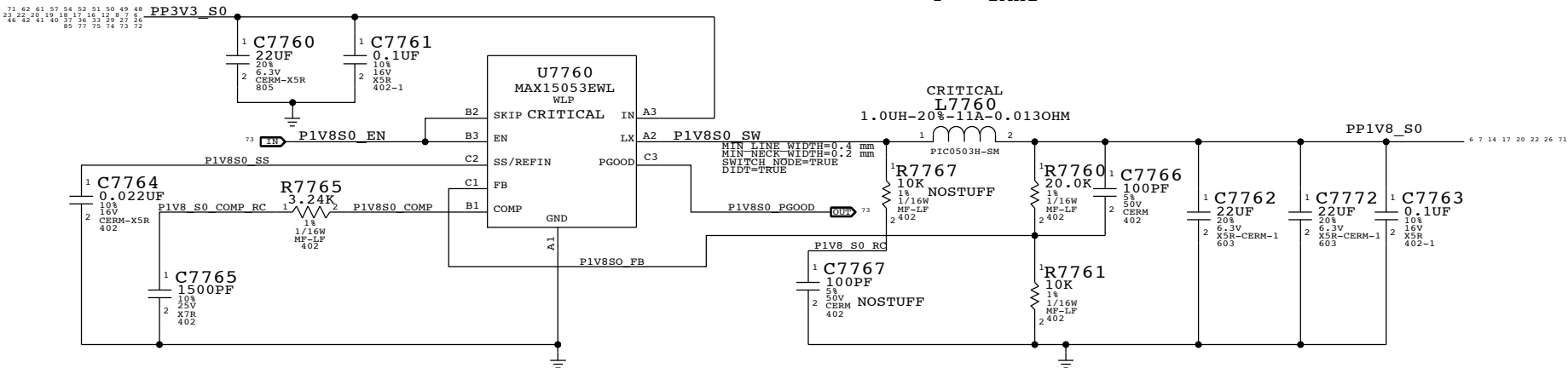
1.05V S5 LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in S5. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



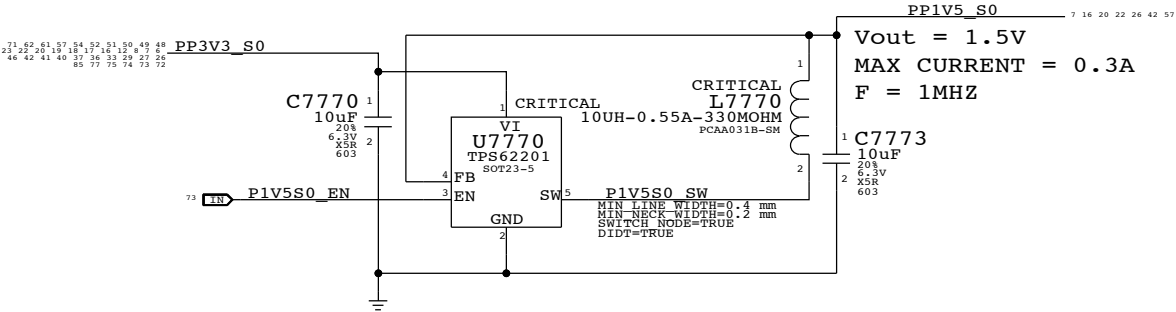
1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



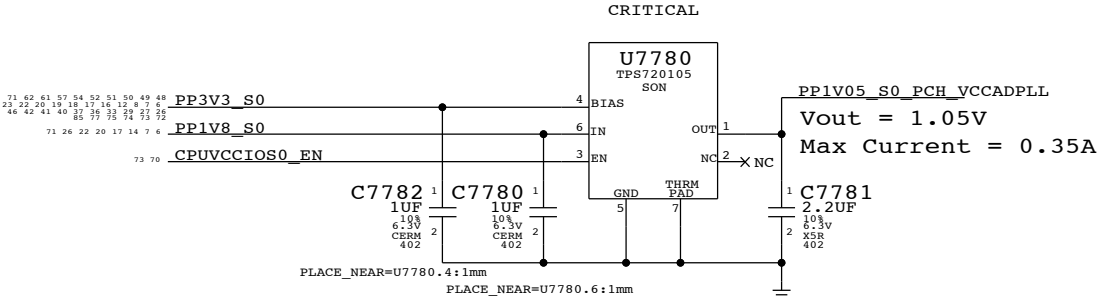
1.5V S0 Switcher


Vout = 1.5V
MAX CURRENT = 0.3A
F = 1MHZ

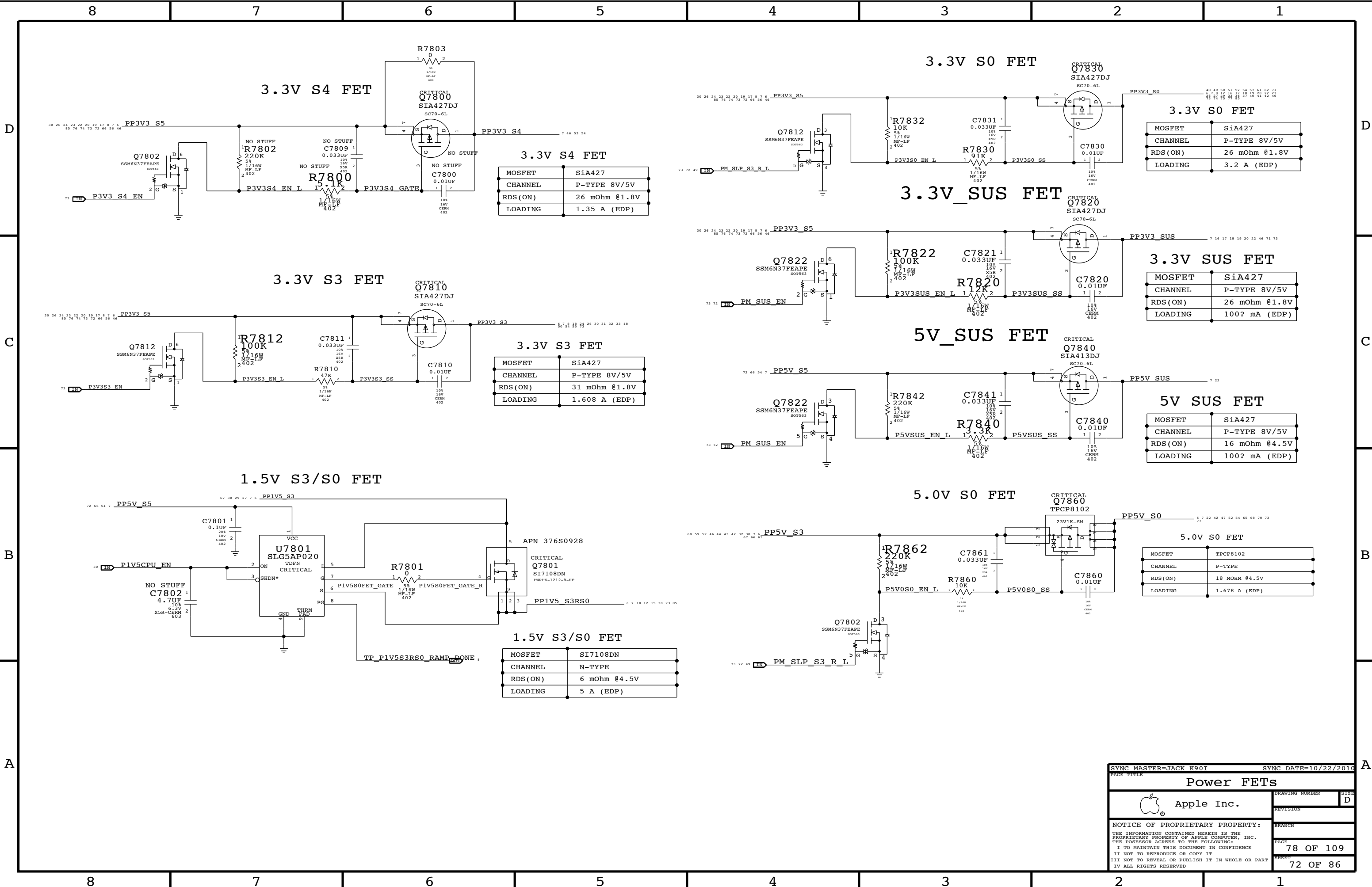


1.05V S0 LDO

Vout = 1.05V
Max Current = 0.35A



SYNC MASTER=JACK K901		SYNC DATE=08/19/2010	
PAGE TITLE			
Misc Power Supplies			
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MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.35 A (EDP)

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	16 mOhm @4.5V
LOADING	100? mA (EDP)

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=JACK K90I

SYNC DATE=10/22/2010

Power FETs

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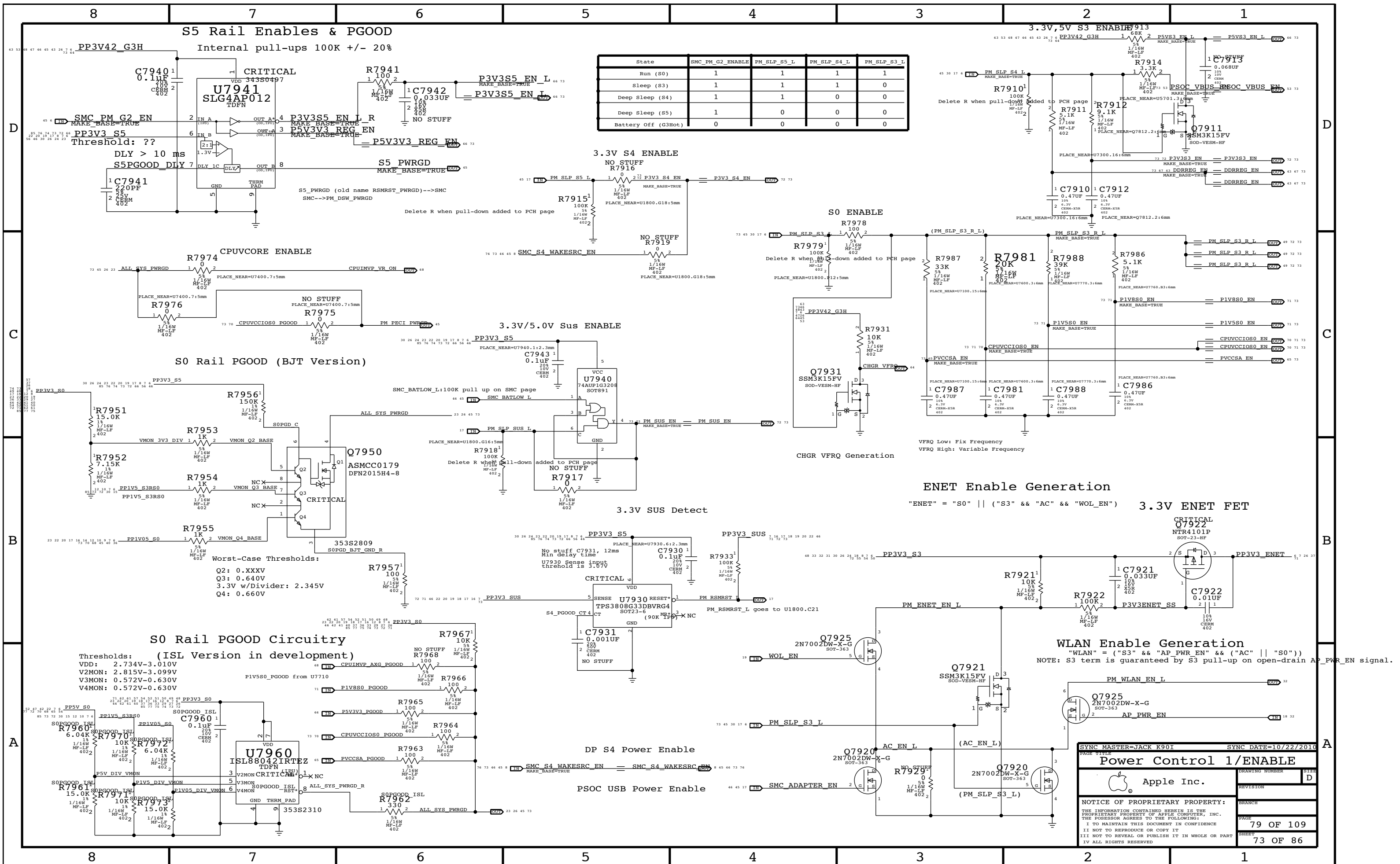
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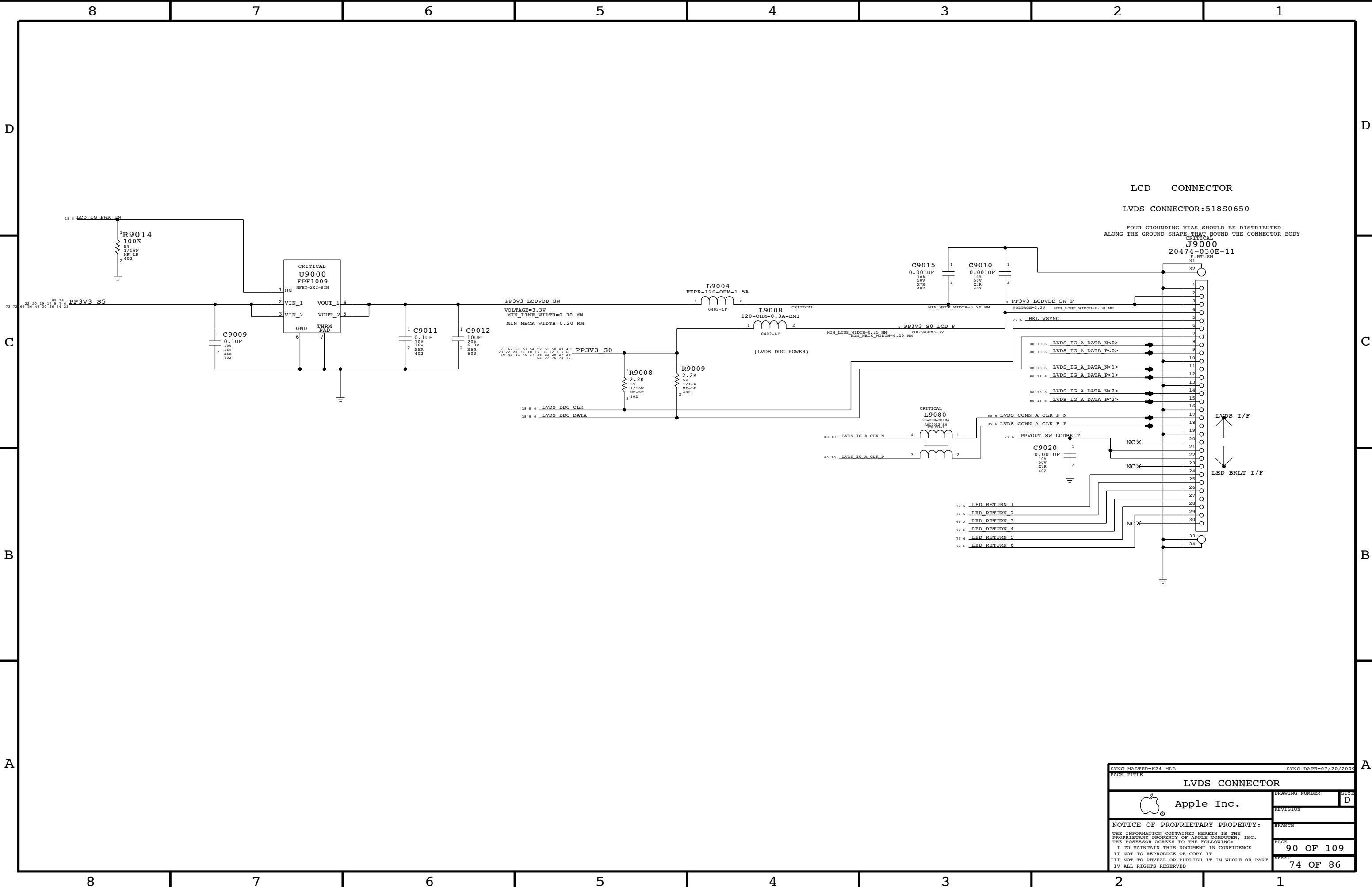
SIZE

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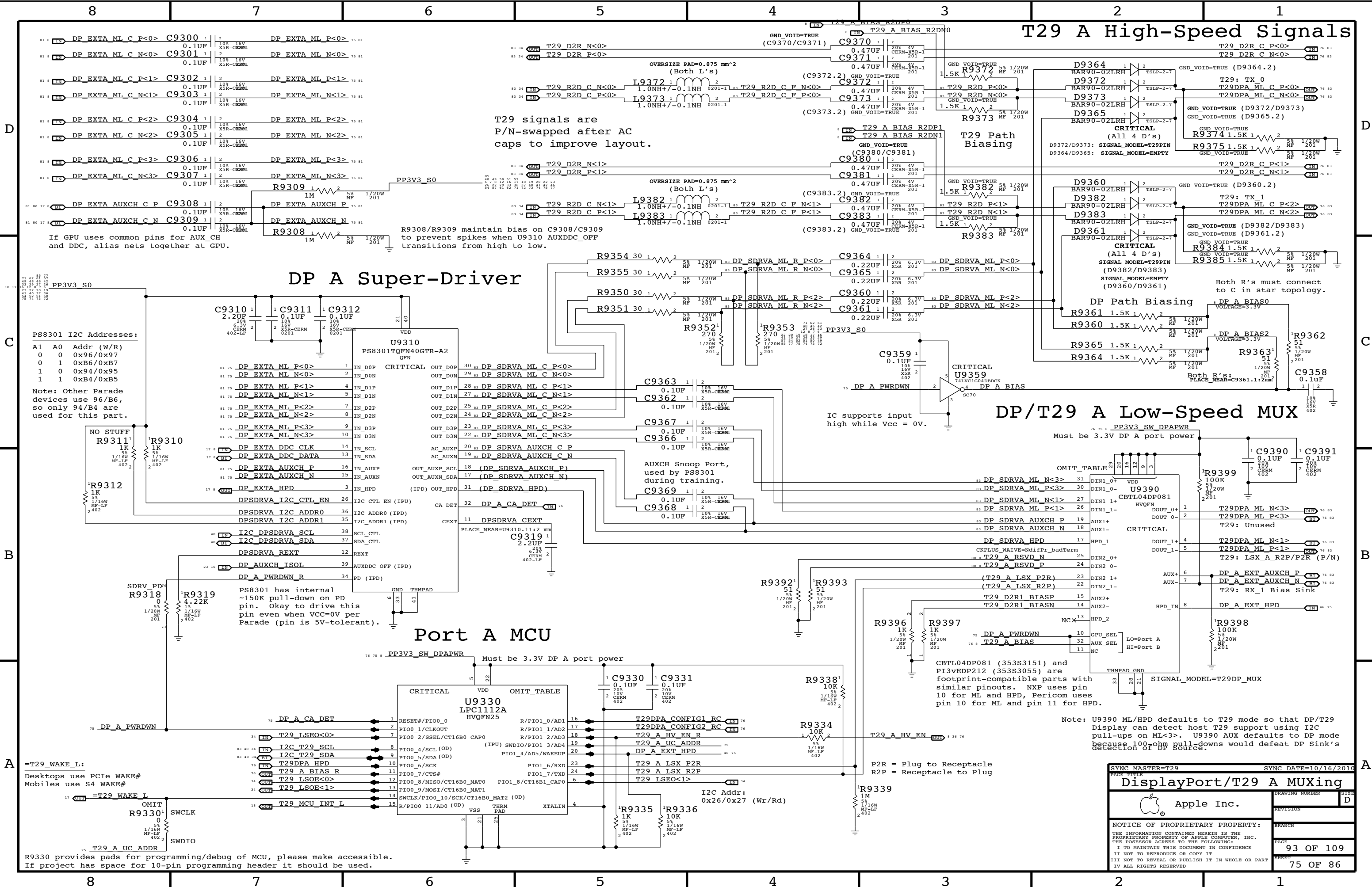
LCD CONNECTOR
LVDS CONNECTOR:518S0650

FOUR GROUNDING VIAS SHOULD BE DISTRIBUTED
ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY

CRITICAL
J9000
20474-030E-11
F-RT-SM

LVDS I/F
LED BKLT I/F

SYNC MASTER=K24 MLB		SYNC DATE=07/20/2009	
PAGE TITLE			
LVDS CONNECTOR			
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D

D

C

C

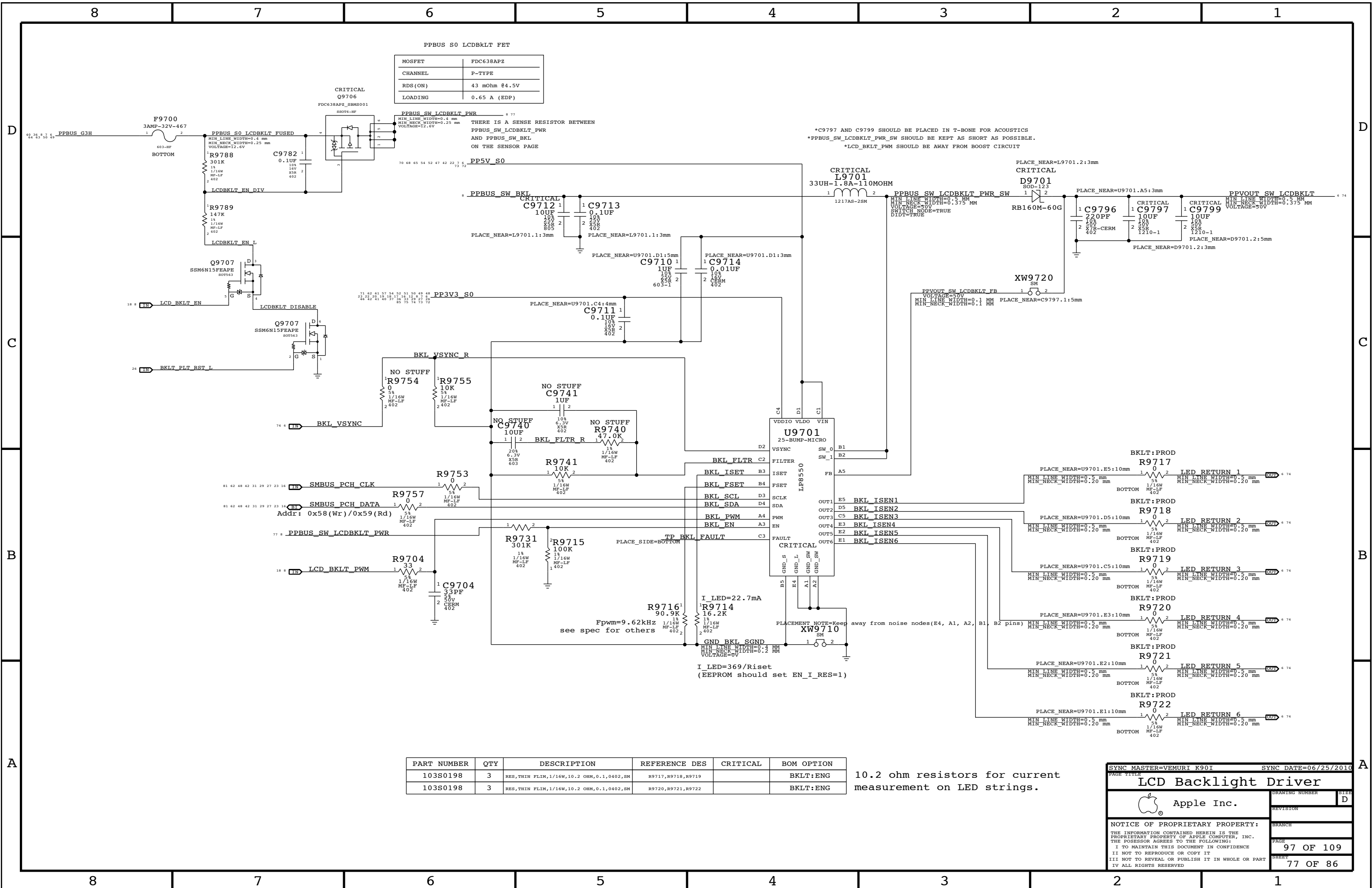
B

B

A


A

PAGE TITLE		SYNC MASTER=T29		SYNC DATE=10/16/2010	
DisplayPort/T29 A MUXing		DRAWING NUMBER		SIZE D	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=VEMURI K901		SYNC DATE=06/25/2010	
PAGE TITLE			
LCD Backlight Driver			
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D

C

B

A

D

C

B

A

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for IbeX Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for IbeX Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

DisplayPort Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?

PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

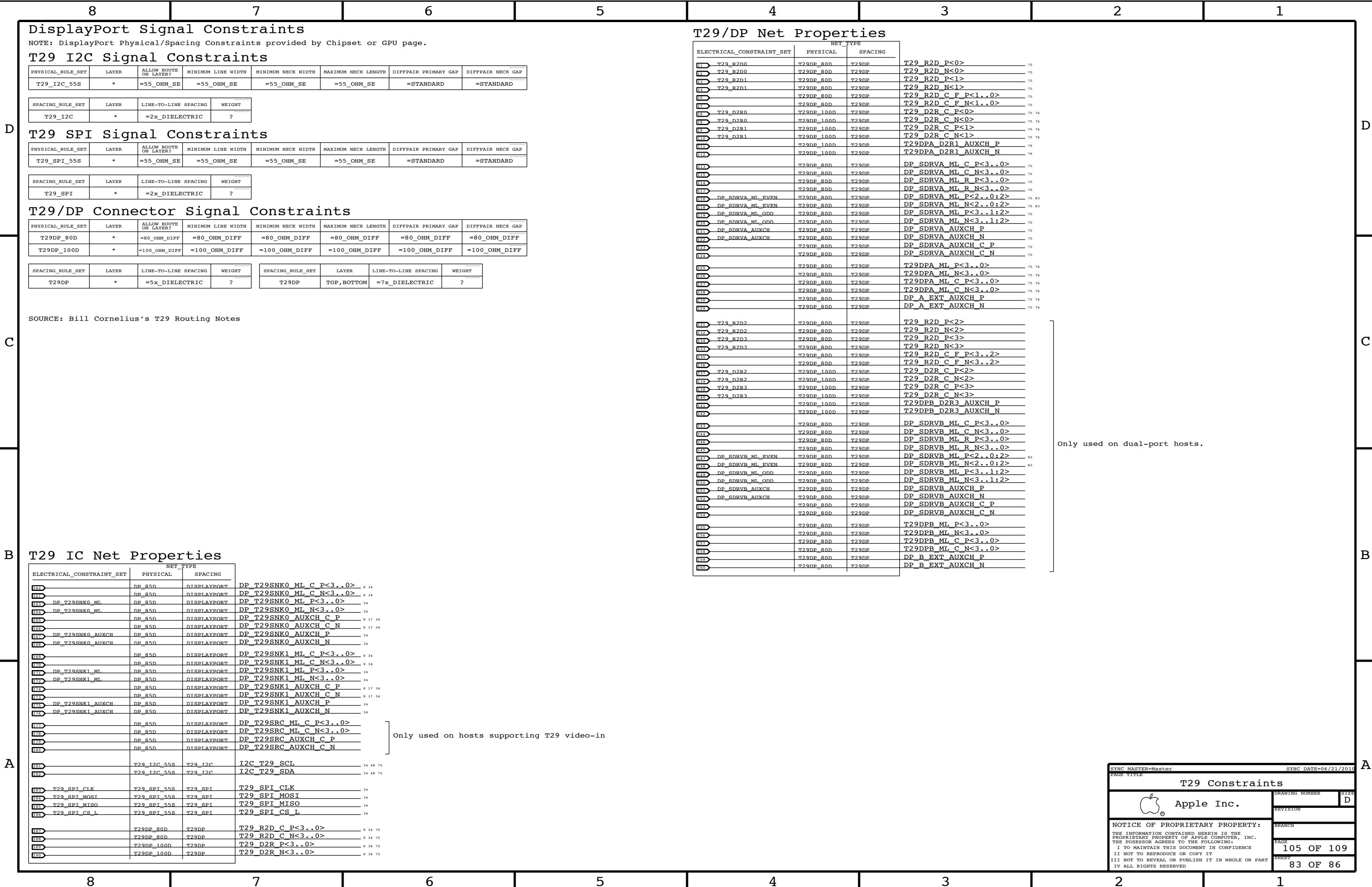
ELECTRICAL_CONSTRAINT_SET		NET_TYPE	
	PHYSICAL	SPACING	
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK
HDA_BIT_CLK_R	HDA_50S	HDA	HDA_BIT_CLK_R
HDA_SYNC	HDA_50S	HDA	HDA_SYNC
HDA_SYNC_R	HDA_50S	HDA	HDA_SYNC_R
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L
HDA_RST_L	HDA_50S	HDA	HDA_RST_L
HDA_SDIO0	HDA_50S	HDA	HDA_SDIO0
HDA_SDIO0	HDA_50S	HDA	AUD_SDI_R
HDA_SDO0T	HDA_50S	HDA	HDA_SDO0T
HDA_SDO0T	HDA_50S	HDA	HDA_SDO0T_R
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK
SPI_CLK	SPI_55S	SPI	SPI_CLK_R
SPI_CLK	SPI_55S	SPI	SPI_CLK
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R
SPI_MOSI	SPI_55S	SPI	SPI_MOSI
SPI_MISO	SPI_55S	SPI	SPI_MISO
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L
SPI_CS0	SPI_55S	SPI	SPI_CS0_L
PCIE_ENET_R2D_P	PCIE_85D	PCIE	PCIE_ENET_R2D_P
PCIE_ENET_R2D_N	PCIE_85D	PCIE	PCIE_ENET_R2D_N
PCIE_ENET_R2D_C_P	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N
PCIE_ENET_D2R_P	PCIE_85D	PCIE	PCIE_ENET_D2R_P
PCIE_ENET_D2R_N	PCIE_85D	PCIE	PCIE_ENET_D2R_N
PCIE_ENET_D2R_C_P	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P
PCIE_ENET_D2R_C_N	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N
PCIE_AP_R2D_P	PCIE_85D	PCIE	PCIE_AP_R2D_P
PCIE_AP_R2D_N	PCIE_85D	PCIE	PCIE_AP_R2D_N
PCIE_AP_R2D_C_P	PCIE_85D	PCIE	PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N	PCIE_85D	PCIE	PCIE_AP_R2D_C_N
PCIE_AP_D2R_P	PCIE_85D	PCIE	PCIE_AP_D2R_P
PCIE_AP_D2R_N	PCIE_85D	PCIE	PCIE_AP_D2R_N
PCIE_FW_R2D_P	PCIE_85D	PCIE	PCIE_FW_R2D_P
PCIE_FW_R2D_N	PCIE_85D	PCIE	PCIE_FW_R2D_N
PCIE_FW_R2D_C_P	PCIE_85D	PCIE	PCIE_FW_R2D_C_P
PCIE_FW_R2D_C_N	PCIE_85D	PCIE	PCIE_FW_R2D_C_N
PCIE_FW_D2R_P	PCIE_85D	PCIE	PCIE_FW_D2R_P
PCIE_FW_D2R_N	PCIE_85D	PCIE	PCIE_FW_D2R_N
PCIE_FW_D2R_C_P	PCIE_85D	PCIE	PCIE_FW_D2R_C_P
PCIE_FW_D2R_C_N	PCIE_85D	PCIE	PCIE_FW_D2R_C_N
PCIE_AP_D2R_PI_P	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P
PCIE_AP_D2R_PI_N	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N
PCIE_AP_R2D_PI_P	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P
PCIE_AP_R2D_PI_N	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N
NC_PEG_CLK100MP	CLK_PCIE_90D	CLK_PCIE	NC_PEG_CLK100MP
NC_PEG_CLK100MN	CLK_PCIE_90D	CLK_PCIE	NC_PEG_CLK100MN
PCIE_CLK100M_ENET_P	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N
PCIE_CLK100M_AP_P	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N
PCIE_CLK100M_FW_P	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P
PCIE_CLK100M_FW_N	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N
NC_PCIE_CLK100M_EXCARDP	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARDP
NC_PCIE_CLK100M_EXCARDN	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARDN
PCH_VSS_NCTF<1>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<1>
PCH_VSS_NCTF<2>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<2>
PCH_VSS_NCTF<5>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<5>
TP_PCH_VSS_NCTF<7>	CHU_27F4S	CHU_COMP	TP_PCH_VSS_NCTF<7>
PCH_VSS_NCTF<9>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<9>
PCH_VSS_NCTF<9>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<9>
PCH_VSS_NCTF<11>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<11>
PCH_VSS_NCTF<12>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<12>
PCH_VSS_NCTF<15>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<15>
PCH_VSS_NCTF<17>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<17>
PCH_VSS_NCTF<19>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<19>
PCH_VSS_NCTF<21>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<21>
PCH_VSS_NCTF<22>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<22>
PCH_VSS_NCTF<25>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<25>
PCH_VSS_NCTF<27>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<27>
PCH_VSS_NCTF<29>	CHU_27F4S	CHU_COMP	PCH_VSS_NCTF<29>

Chipset Net Properties

ELECTRICAL CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP30 DP_EXTN_ML	DP_85D	DISELAYPORT	DP_EXTN_ML C P<3..0>	8 75
DP30 DP_EXTN_ML	DP_85D	DISELAYPORT	DP_EXTN_ML C N<3..0>	8 75
DP30 DP_EXTN_ML	DP_85D	DISELAYPORT	DP_EXTN_ML P<3..0>	75
DP30 DP_EXTN_ML	DP_85D	DISELAYPORT	DP_EXTN_ML N<3..0>	75
DP30 DP_EXTN_AUXCH	DP_85D	DISELAYPORT	DP_EXTN_AUXCH C P	8 17 75
DP30 DP_EXTN_AUXCH	DP_85D	DISELAYPORT	DP_EXTN_AUXCH C N	8 17 75
DP30 DP_EXTN_AUXCH	DP_85D	DISELAYPORT	DP_EXTN_AUXCH P	75
DP30 DP_EXTN_AUXCH	DP_85D	DISELAYPORT	DP_EXTN_AUXCH N	75
DP30 DP_INT_ML	DP_85D	DISELAYPORT	DP_INT_ML C P<3..0>	
DP30 DP_INT_ML	DP_85D	DISELAYPORT	DP_INT_ML C N<3..0>	
DP30 DP_INT_AUXCH	DP_85D	DISELAYPORT	DP_INT_AUXCH C P	
DP30 DP_INT_AUXCH	DP_85D	DISELAYPORT	DP_INT_AUXCH C N	
DP30 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D C P<3..0>	8 34
DP30 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D C N<3..0>	8 34
DP30 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D P<3..0>	34
DP30 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D N<3..0>	34
DP30 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R P<3..0>	8 34
DP30 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R N<3..0>	8 34
DP30 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R C P<3..0>	34
DP30 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R C N<3..0>	34
DP30 PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 P	16 34
DP30 PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 N	16 34

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
IP2R1	<u>SYSCCLK_CLK32K_RTC</u>	CLK_SLOW_55R	CLK_SLOW	<u>SYSCCLK_CLK32K_RTC</u>	16 26
IP2R2	<u>SYSCCLK_CLK25M_SB</u>	CLK_25M_55R	CLK_25M	<u>SYSCCLK_CLK25M_SB</u>	16 26
IP2R3	<u>SYSCCLK_CLK25M_SB_R</u>	CLK_25M_55R	CLK_25M	<u>SYSCCLK_CLK25M_SB_R</u>	16
IP2R4	<u>SYSCCLK_CLK25M_ENET</u>	CLK_25M_55R	CLK_25M	<u>SYSCCLK_CLK25M_ENET</u>	26 37
IP2R5	<u>SYSCCLK_CLK25M_ENET_R</u>	CLK_25M_55R	CLK_25M	<u>SYSCCLK_CLK25M_ENET_R</u>	
IP2R6	<u>SYSCCLK_CLK25M_T29</u>	CLK_25M_55R	CLK_25M	<u>SYSCCLK_CLK25M_T29</u>	26 34
IP2R7	<u>SYSCCLK_CLK25M_T29_R</u>	CLK_25M_55R	CLK_25M	<u>SYSCCLK_CLK25M_T29_R</u>	34



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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 IC Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
H02	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0> 8 34
H04	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0> 8 34
H05	DP_T29SNK0_ML	DISPLAYPORT	DP_T29SNK0_ML_P<3..0> 34
H06	DP_T29SNK0_ML	DISPLAYPORT	DP_T29SNK0_ML_N<3..0> 34
H07	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P 8 17 34
H08	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N 8 17 34
H09	DP_T29SNK0_AUXCH	DISPLAYPORT	DP_T29SNK0_AUXCH_P 34
H10	DP_T29SNK0_AUXCH	DISPLAYPORT	DP_T29SNK0_AUXCH_N 34
H11	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0> 8 34
H12	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0> 8 34
H13	DP_T29SNK1_ML	DISPLAYPORT	DP_T29SNK1_ML_P<3..0> 34
H14	DP_T29SNK1_ML	DISPLAYPORT	DP_T29SNK1_ML_N<3..0> 34
H15	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P 8 17 34
H16	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N 8 17 34
H17	DP_T29SNK1_AUXCH	DISPLAYPORT	DP_T29SNK1_AUXCH_P 34
H18	DP_T29SNK1_AUXCH	DISPLAYPORT	DP_T29SNK1_AUXCH_N 34
H19	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>
H20	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>
H21	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P
H22	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N
H23	T29_T2C_55S	T29_T2C	I2C_T29_SCL 34 48 75
H24	T29_T2C_55S	T29_T2C	I2C_T29_SDA 34 48 75
H25	T29_SPI_CLK	T29_SPI_55S	T29_SPI_CLK 34
H26	T29_SPI_MOSI	T29_SPI_55S	T29_SPI_MOSI 34
H27	T29_SPI_MISO	T29_SPI_55S	T29_SPI_MISO 34
H28	T29_SPI_CS_L	T29_SPI_55S	T29_SPI_CS_L 34
H29	T29DP_80D	T29DP	T29_R2D_C_P<3..0> 8 34 75
H30	T29DP_80D	T29DP	T29_R2D_C_N<3..0> 8 34 75
H31	T29DP_100D	T29DP	T29_D2R_P<3..0> 8 34 75
H32	T29DP_100D	T29DP	T29_D2R_N<3..0> 8 34 75

Only used on hosts supporting T29 video-in

T29 Constraints

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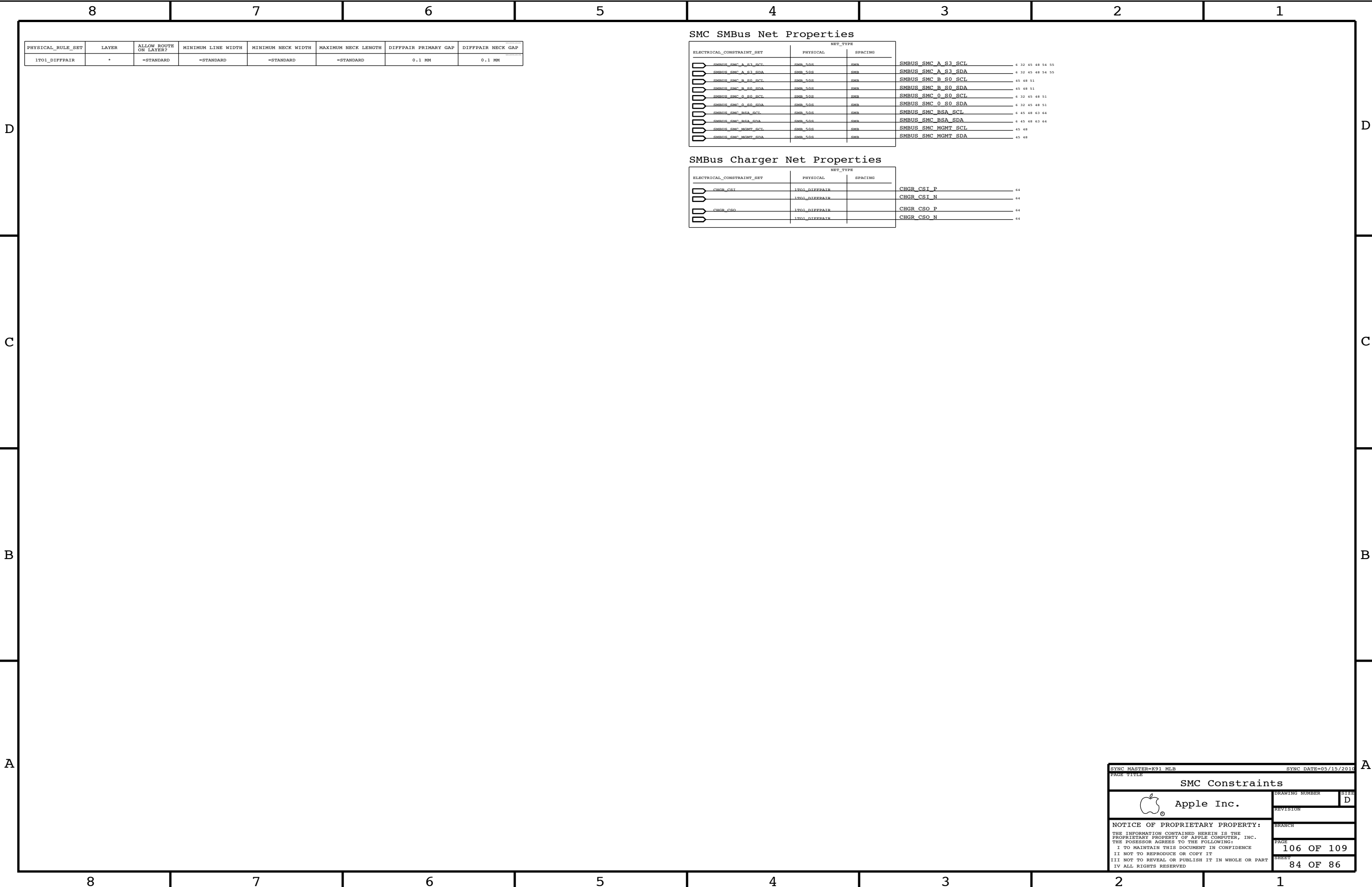
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T29 Constraints

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Apple Inc.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_I701_558	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_I701_558	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	7
THERM	*	=2:1_SPACING	7
AUDIO	*	=2:1_SPACING	7

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENRTPCON	*	25 MILS	2

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	2

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLE	GND	*	GND_P2H8 <small>(Minimum Spacing Rule Set)</small>
MEM_CHD	GND	*	GND_P2H8 <small>(Minimum Spacing Rule Set)</small>
MEM_CTLG	GND	*	GND_P2H8 <small>(Minimum Spacing Rule Set)</small>
MEM_DATA	GND	*	GND_P2H8 <small>(Minimum Spacing Rule Set)</small>
MEM_DQS	GND	*	GND_P2H8 <small>(Minimum Spacing Rule Set)</small>

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	+	GND_P2304
PCIE	GND	+	GND_P2304
SATA	GND	+	GND_P2304
USB	GND	+	GND_P2304
CLK_PCIE	SR_POWER	+	PWR_P2304
SATA	SR_POWER	+	PWR_P2304
USB	SR_POWER	+	PWR_P2304

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

K90i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE	PHYSICAL	SPACING		
			ENET_10G	ENETCONN	ENETCONN P<3,,0>	38
			ENET_10G	ENETCONN	ENETCONN N<3,,0>	38
			SATA_90D	SATA	SATA_ODD_D2R_UF_P	6 42
			SATA_90D	SATA	SATA_ODD_D2R_UF_N	6 42
			SATA_90D	SATA	SATA_HDD_D2R_RDWRV_OUT_P	42
			SATA_90D	SATA	SATA_HDD_D2R_RDWRV_OUT_N	42
			SATA_90D	SATA	SATA_HDD_R2R_RDWRV_IN_P	42
			SATA_90D	SATA	SATA_HDD_R2D_RDWRV_IN_N	42
			SATA_90D	SATA	SATA_HDD_D2R_RDWRV_IN_P	42
			SATA_90D	SATA	SATA_HDD_D2R_RDWRV_IN_N	42
			SATA_90D	SATA	SATA_HDD_R2D_RDWRV_OUT_P	42
			SATA_90D	SATA	SATA_HDD_R2D_RDWRV_OUT_N	42
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUTHERMS D2_P	51
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUTHERMS D2_N	51
			SENSE_DIFFPAIR	SENSE_10G_13G	CPU_THERMD_P	9 51
			SENSE_DIFFPAIR	SENSE_10G_13G	CPU_THERMD_N	9 51
			SENSE_DIFFPAIR	SENSE_10G_13G	T29_THERMD_P	34 51
			SENSE_DIFFPAIR	SENSE_10G_13G	T29_THERMD_N	51
			SENSE_DIFFPAIR	SENSE_10G_13G	T29THERMS D2_P	51
			SENSE_DIFFPAIR	SENSE_10G_13G	T29THERMS D2_N	51
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_HS_COMPUTING_N	50
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_HS_COMPUTING_P	50
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_HS_OTHER_N	50
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_HS_OTHER_P	50
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUVCCIOS0_CS_N	49 70
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUVCCIOS0_CS_P	49 70
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISNS1_P	49 61
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISNS1_N	49 61
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISNS2_P	49 61
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISNS2_N	49 61
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISNSIG_P	49 61
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISNSIG_N	49 61
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISUM_R_P	49
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISUM_R_N	49
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISUMG_R_P	49
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISUMG_R_N	49
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISNS_P	49
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISNS_N	49
			SENSE_DIFFPAIR	SENSE_10G_13G	VCCRAS0_CS_P	65
			SENSE_DIFFPAIR	SENSE_10G_13G	VCCRAS0_CS_N	65
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISUMG_P	68 61
			SENSE_DIFFPAIR	SENSE_10G_13G	CPUI MVP ISUMG_N	68 61
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_CPU_N	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_CPU_P	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_HDD_N	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_HDD_P	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_HDD_R_N	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_HDD_R_P	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_LCDRKIT_N	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_LCDRKIT_P	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_ODD_N	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_ODD_P	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_ODD_R_N	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_ODD_R_P	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_P1VBGPU_N	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_P1VBGPU_P	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_P1VBGPU_R_N	
			SENSE_DIFFPAIR	SENSE_10G_13G	ISNS_P1VBGPU_R_P	
			LVDS_00D	LVDS	LVDS_CONN_A_CLK_F_N	6 74
			LVDS_00D	LVDS	LVDS_CONN_A_CLK_F_P	6 74


K90i Specific Net Properties

[illegible]

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

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Project Specific Constraints			
 Apple Inc.		DRAWING NUMBER	SIZE D
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K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TFIF, BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OH_0E	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OH_0E	*	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OH_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
40_OH_SE	ISL10	N	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OH_SE	ISL3, ISL4, ISL9	Y	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OH_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OH_SE	TOP,BOTTOM	Y	0.190 MM	0.1 MM			
37_OH_SE	ISL10	N	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OH_SE	ISL3,ISL4,ISL9	Y	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OH_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.235 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_00H_02	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_00H_02	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL9, ISL4, ISL9	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	ISL10	N	0.140MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
\$S_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
\$S_OHM_DIFF	ISL3, ISL4	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
\$S_OHM_DIFF	ISL9, ISL10	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
\$S_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.1 MM	0.190 MM	0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL9, ISL4	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.111 MM	0.111 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	1SL4, 1SL4	Y	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	1SL9, 1SL10	Y	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
48_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	1SL3, 1SL4	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	1SL9, 1SL10	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P10M	*	=DEFAULT	?
BGA_P20M	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
"	"	BGA	BGA_P10M
MEM_CLK	"	BGA	BGA_P20M
CLK_PCIE	"	BGA	BGA_P30M
CLK_BLOW	"	BGA	BGA_P20M

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:5:1_SPACING	*	0.15 MM	2
2:1:1_SPACING	*	0.2 MM	2
2:5:1_SPACING	*	0.25 MM	2
3:1:1_SPACING	*	0.3 MM	2
4:1:1_SPACING	*	0.4 MM	2

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_NGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_NGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_NGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.